

COMPAL CONFIDENTIAL

MODEL NAME : LOKI 15/17  
PCB NO : DA6001TR010  
BOM P/N : 431A7X31L01~L07

KBL-U & R + MEC1416 board  
2017-07-26  
REV : 1.0 (A00)

ZZZ

DAZ21Q00101

PCB@

PCB CAL60 LA-F114P LS-F111P GOLD A31 !

SKL

UC1

SKL\_U

SA0000ACL1L

i3SKL\_2.0G\_SMB0@

S IC FJ8066201931106 SR2UW D1 2G A31!

KBL

UC1

KBL\_U\_Celeron

SA0000ADL3L

KBL\_U\_Celeron@

S IC FJ8067702739933 SR349 H0 1.8G A31!

UC1

KBL\_U\_Pentium

SA0000ADV3L

KBL\_U\_Pentium@

S IC FJ8067702739932 SR348 H0 2.3G A31!

UC1

KBL\_U\_i3

SA0000A380L

KBL\_U\_i3@

S IC A31 FJ8067702739738 QLDP H0 2.4G

UC1

KBL\_R\_i5

SA0000AWB3L

i5KBLR\_1.6G\_QS@

S IC FJ8067703282221 SR3LB Y0 1.6G A31!

UC1

KBL\_R\_i7

SA0000AQZ0L

i7KBLR\_1.8G\_ES@

S IC A31 FJ8067703281813 QN5C Y0 1.8G

UC1

KBL\_R\_i7

SA0000AWC2L

i7KBLR\_1.8G\_QS@

S IC FJ8067703281816 SR3LC Y0 1.8G A31!

UC1


KBL\_U\_i3

SA0000B2Y1L

i3KBLU\_2.7G\_QS@

S IC FJ8067702739765 SR3JY H0 2.7G A31!

Layout Dell logo



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REV: X00  
PWB: 9HTP8

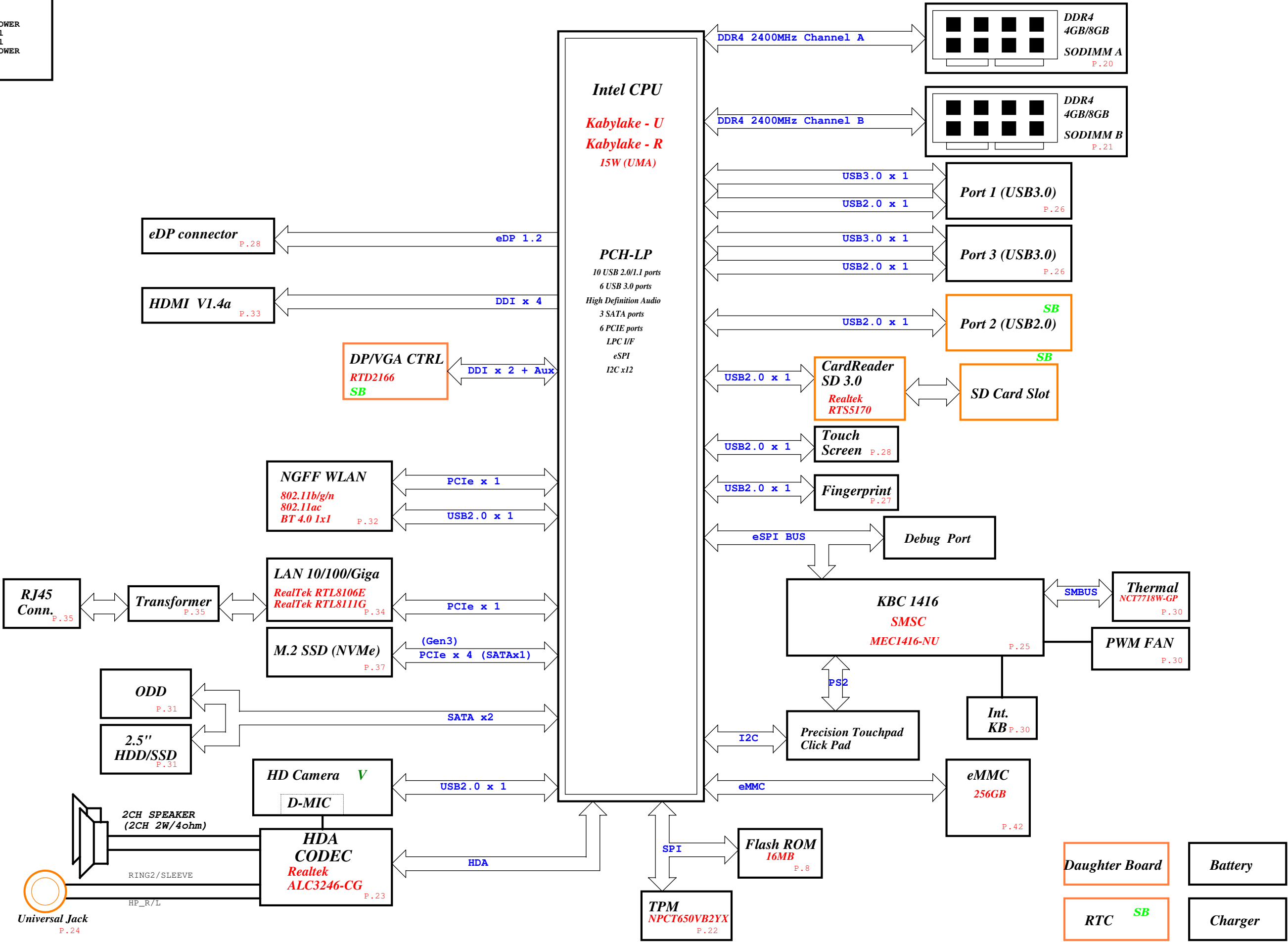
@ : Un-pop Component  
UMA@/DIS@ : UMA & DIS Type  
U22@/U42@ : KBL U/KBL U-R  
EC@ : EC  
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
TP\_WAKE@/NTP\_WAKE@ : TouchPad wake  
KBBL@ : KB Backlight  
TPM@/FTPM@ : HW TPM/SW TPM  
MMC@ : eMMC  
FFS@ : Free Fall Sensor  
MODS@ : Modern Standby

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				Rev	A00

PCB Stack
1.0mm/6L
L1:TOP L2:GND/POWER L3:Signal L4:Signal L5:GND/POWER L6:BOT

# Block Diagram



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## POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB2.0 Port1
2	USB2.0 Port2 , IO/B
3	USB2.0 Port3
4	NC
5	CCD
6	Card Reader IO/B
7	BT
8	Touch Screen
9	Finger Printer
10	NC

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 Port1
USB3.0-2			NC
USB3.0-3			USB3.0 Port3
USB3.0-4			NC
USB3.0-5	PCIE-1		NC
USB3.0-6	PCIE-2		NC
	PCIE-3		NC
	PCIE-4		NC
	PCIE-5		10/100M LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

## PM TABLE

<div>power plane</div> <div>State</div>	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM  +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST  +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG  +VCC_GT +VCC_SA  +VGA_CORE +VCC_CORE  +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

## Board ID table

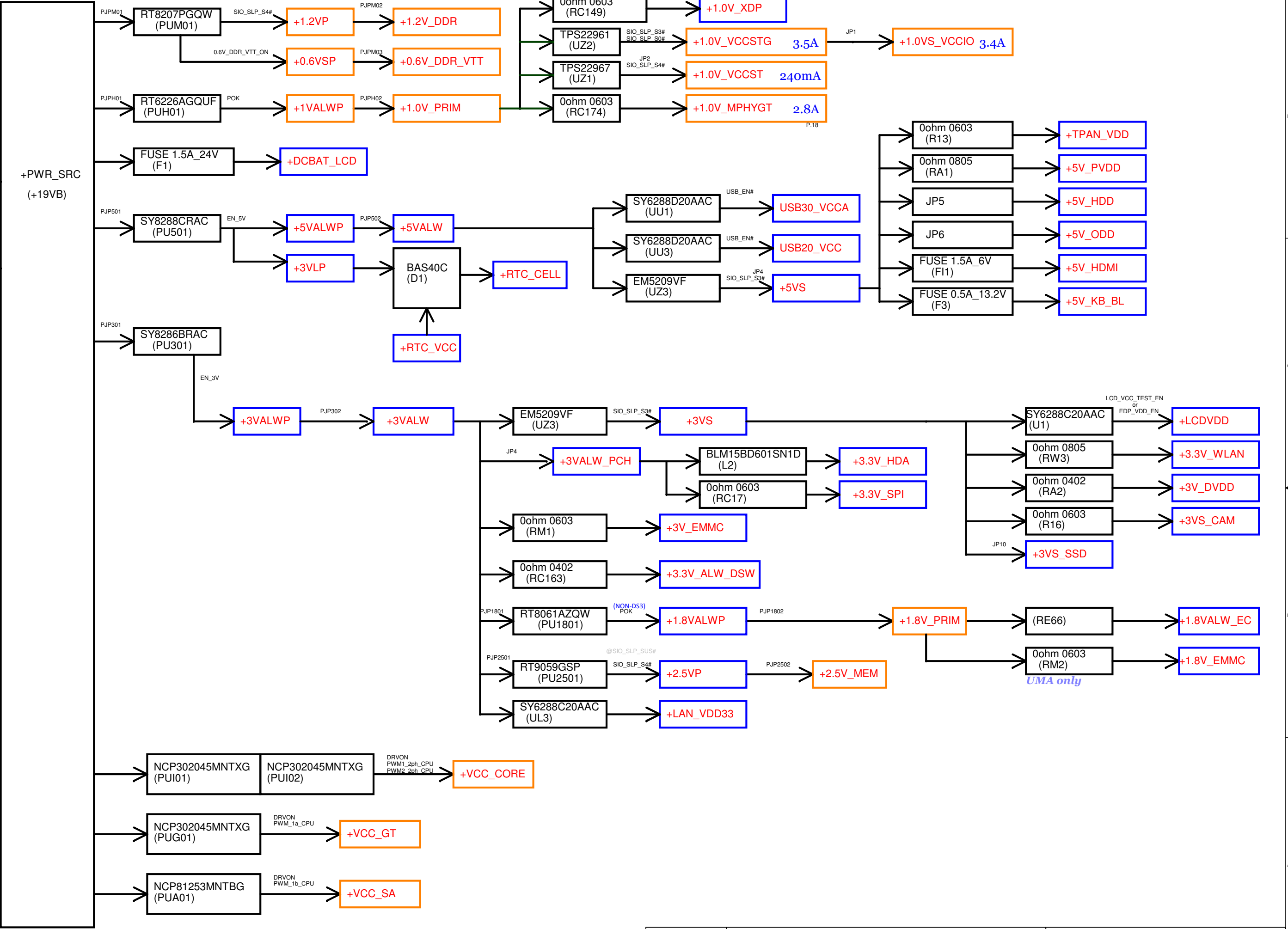
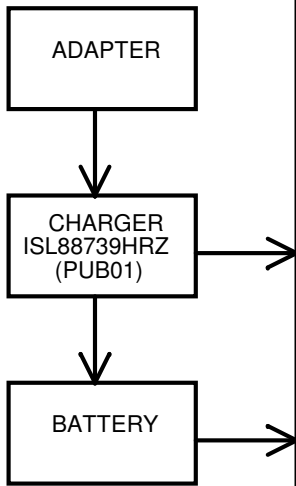
Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	EVT
2	100	17.8K	2.801	DVT1
3	100	27K	2.598	DVT2
4	100	37.4K	2.402	
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	
11	100	TBD	0.9	
12	100	TBD	0.7	
13	100	TBD	0.5	
14	100	TBD	0.3	

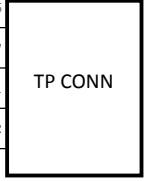
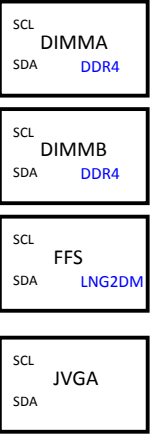
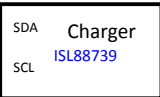
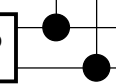
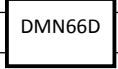
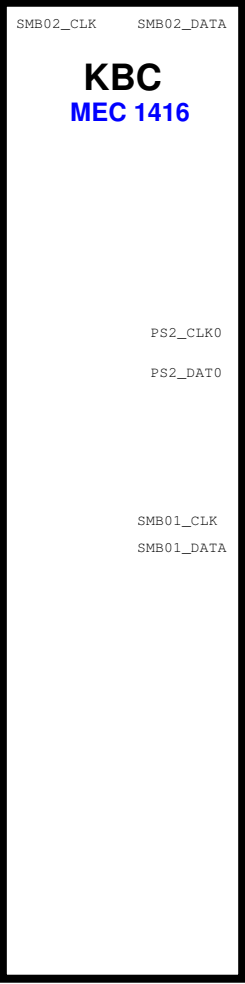
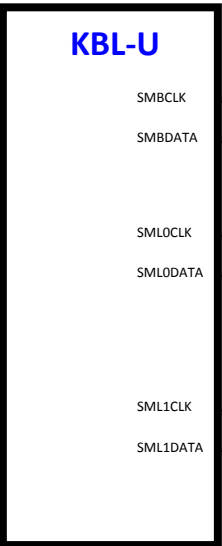
## High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
USB3 #1 (Capable of OTG)	USB3 #2	SSIC	USB3 #3	USB3 #4	USB3 #5	USB3 #6	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12
	X2				X4	X2		X2	X2		X4	X2		X2		
															X2	X4
Intel® RST for PCIe Storage Device #1				Intel® RST for PCIe Storage Device #2												

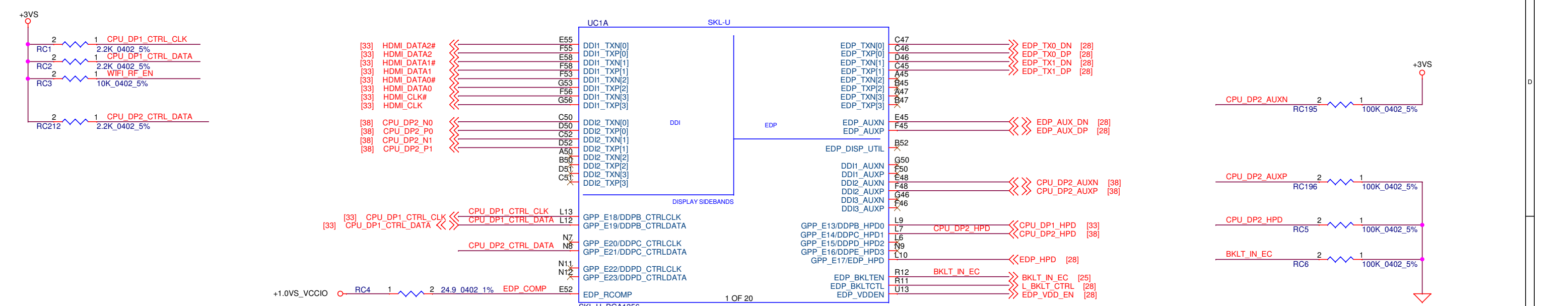
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CPU PWR  
Peripheral Device PWR





Main Func = CPU

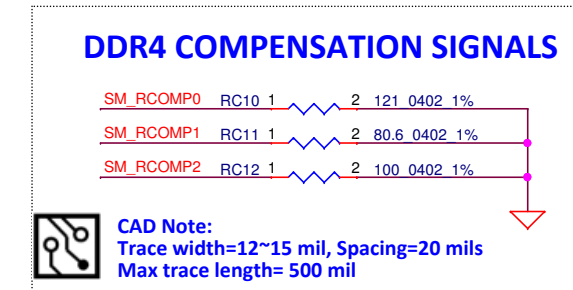
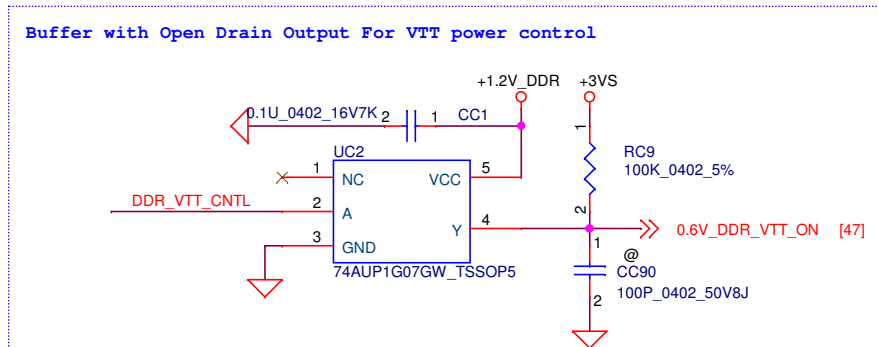
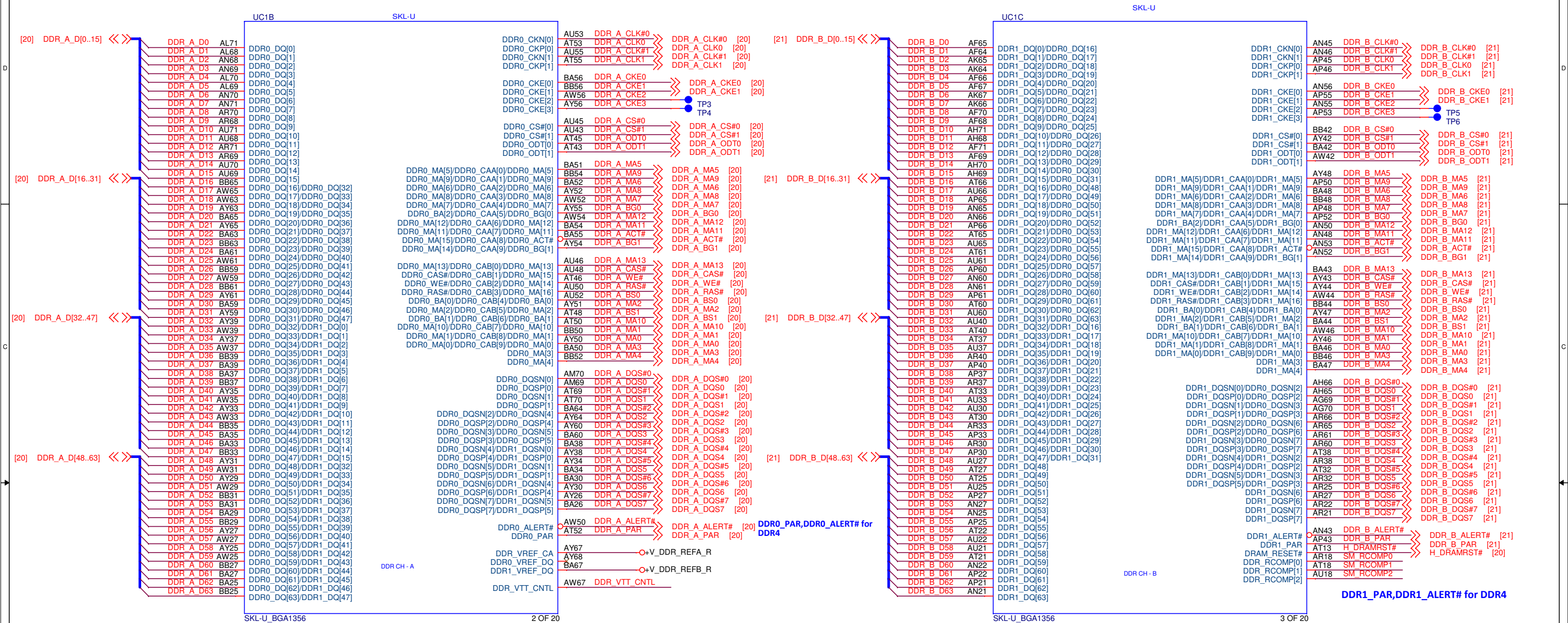


**COMPENSATION PU FOR eDP**  
CAD Note:Min trace width=20 mils ,Spacing=25mil,  
Max length=100 mils.

**SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0**

# Main Func = CPU

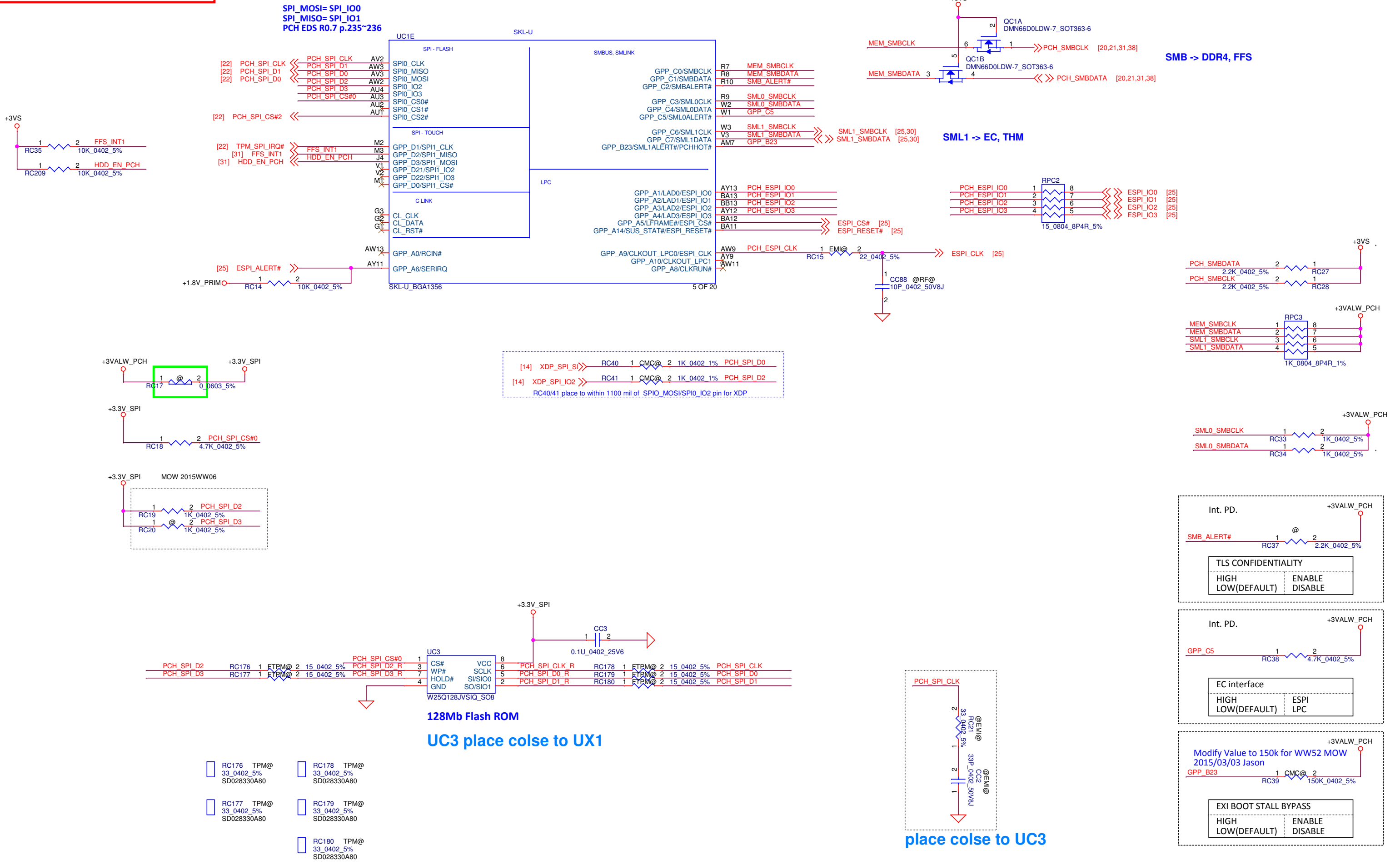
## DDR4 Interleaved Memory



**CAD Note:**  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

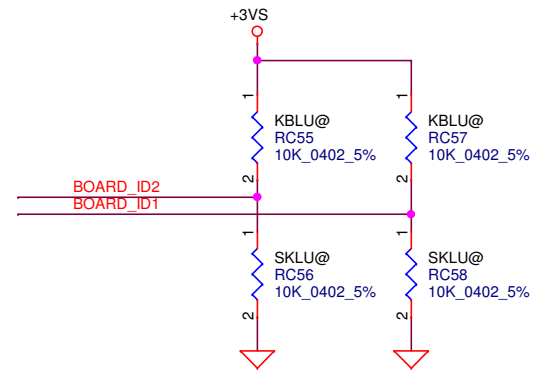
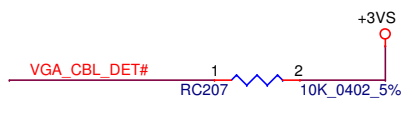
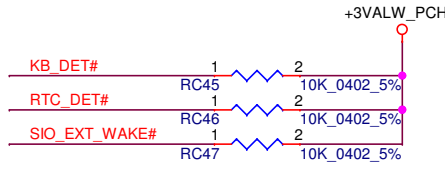
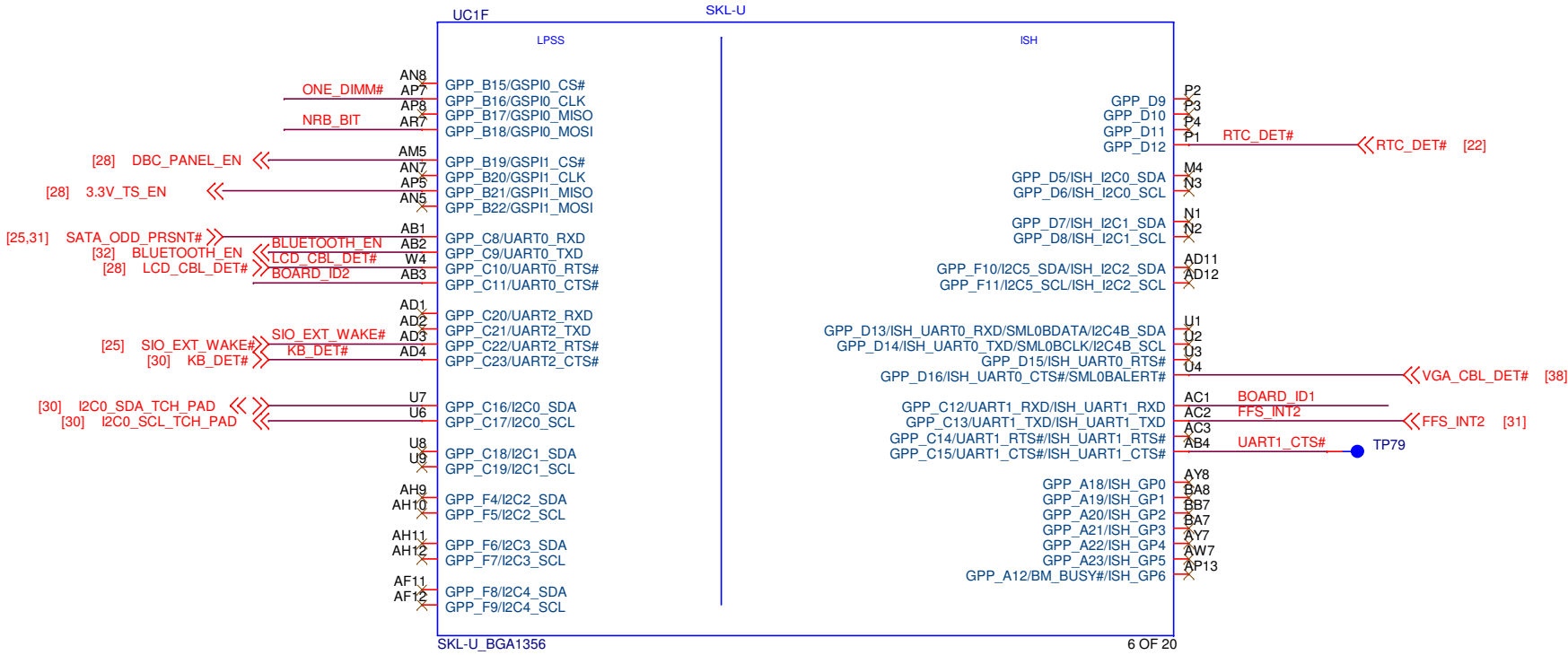
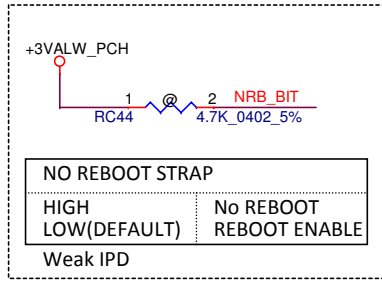
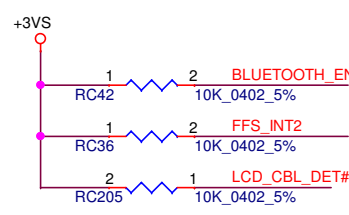
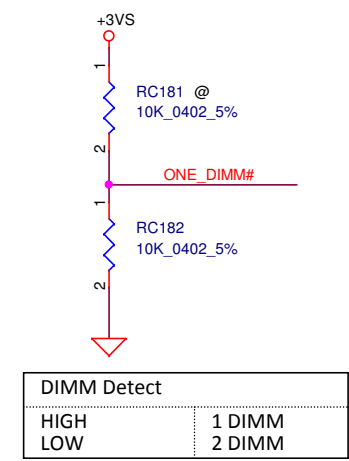
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Main Func = CPU



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Main Func = CPU

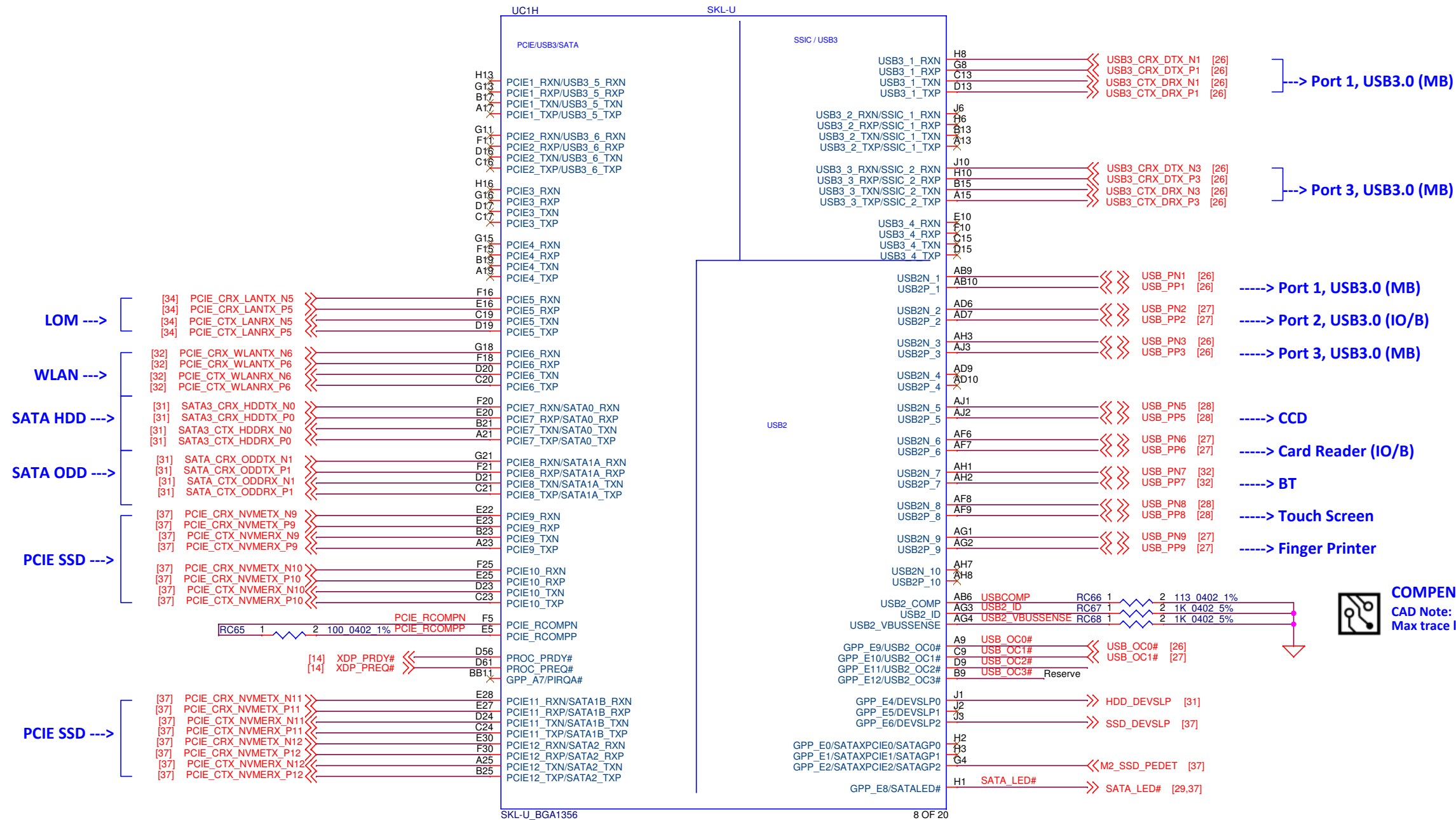


CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

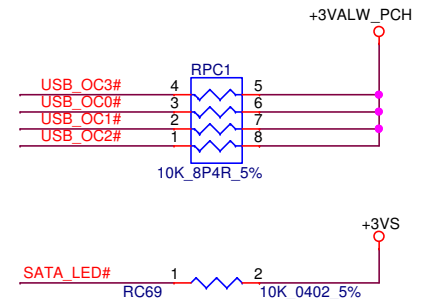
RC55 KBLR@  
10K\_0402\_5%  
SD028100280

RC58 KBLR@  
10K\_0402\_5%  
SD028100280

Main Func = CPU

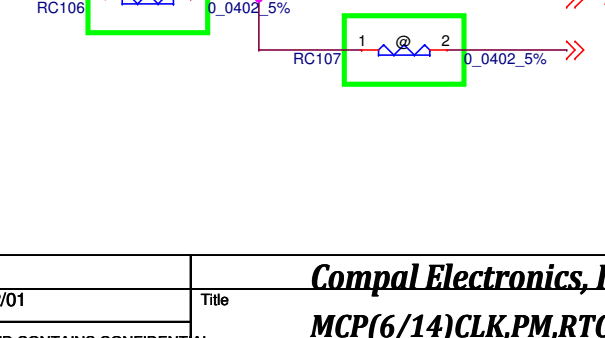
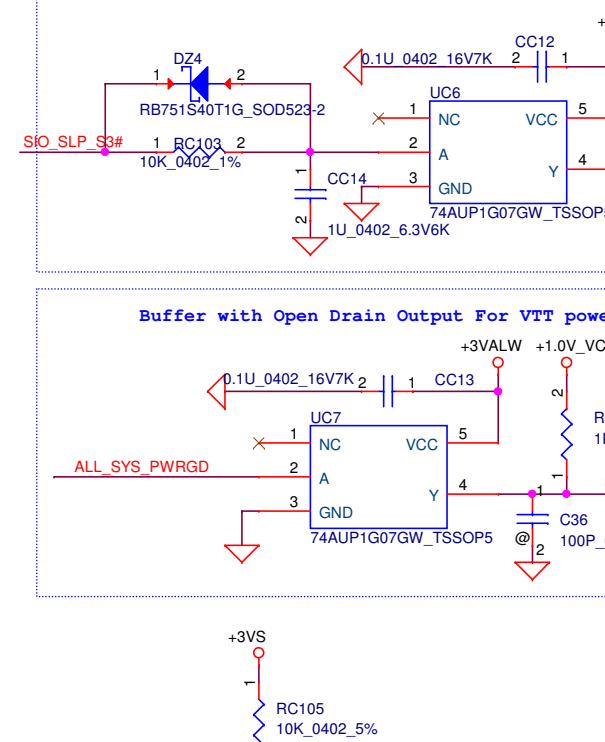
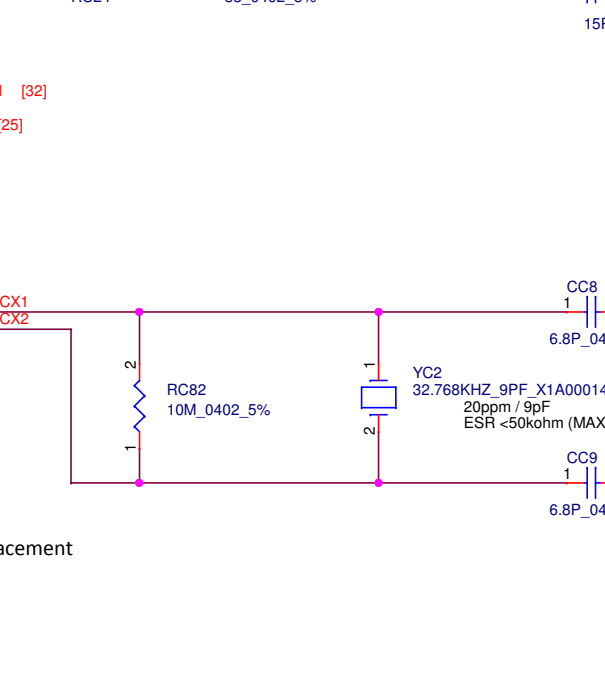
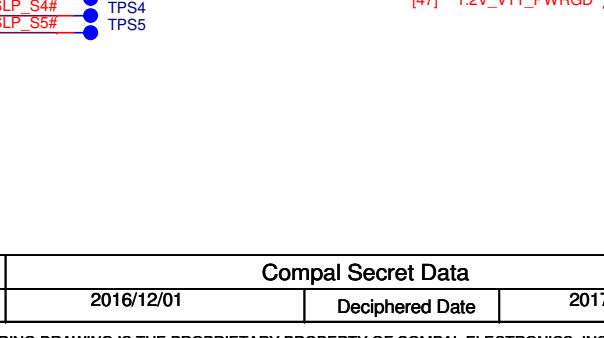
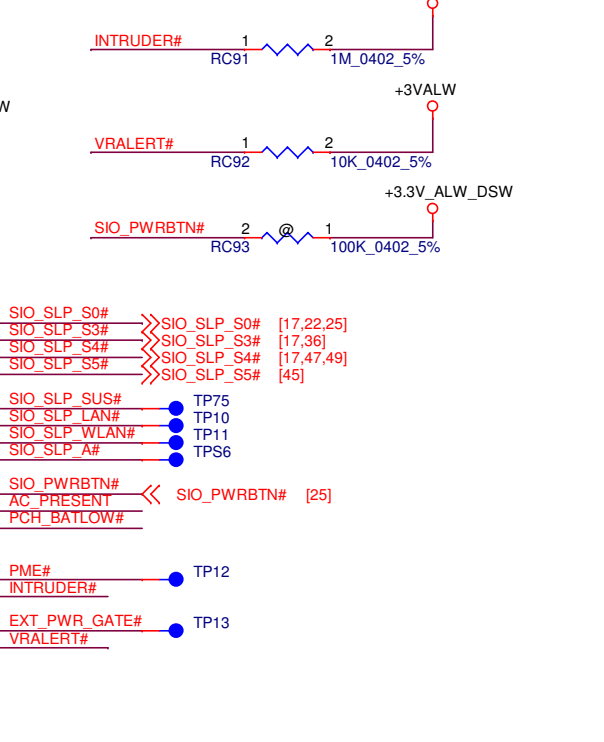
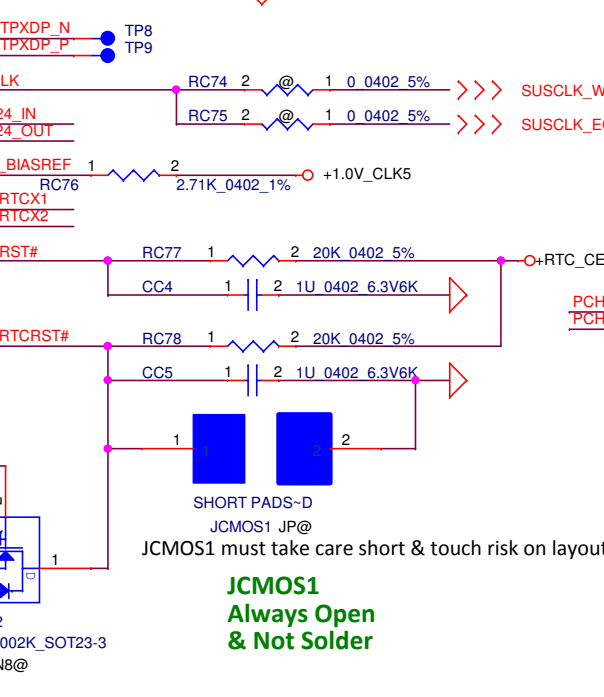
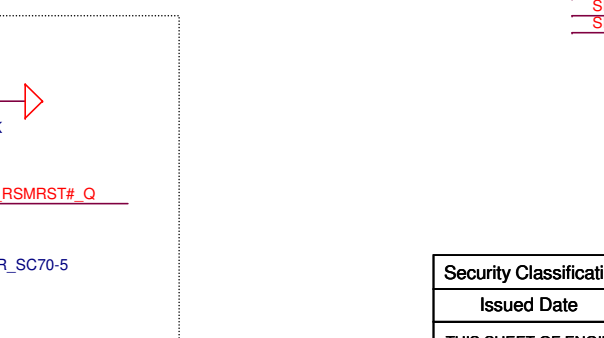
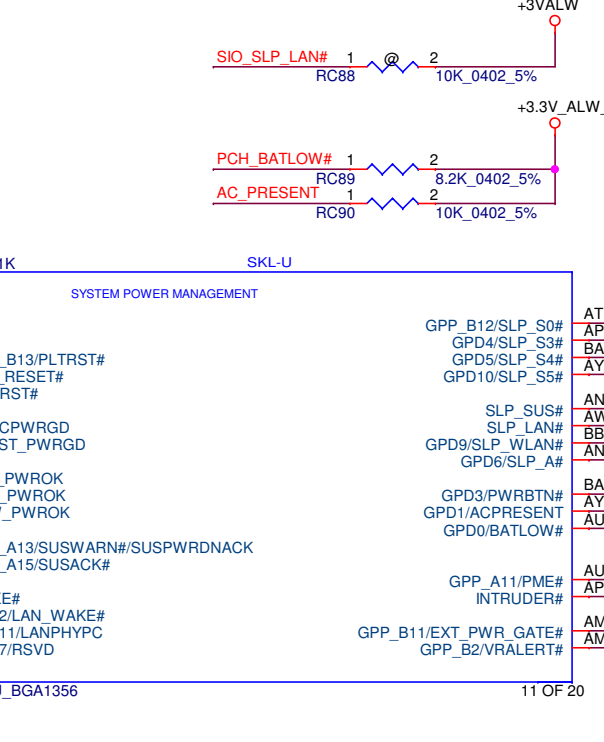
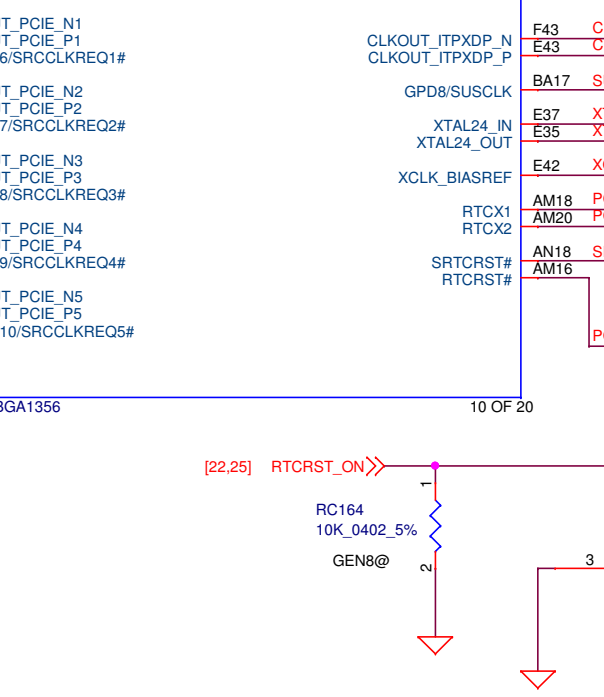
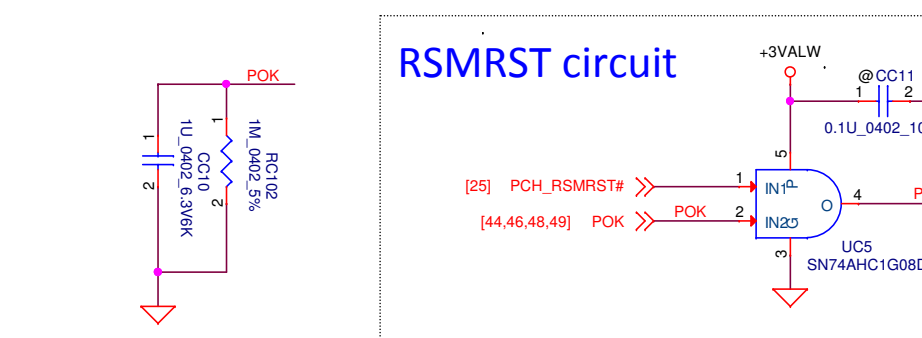
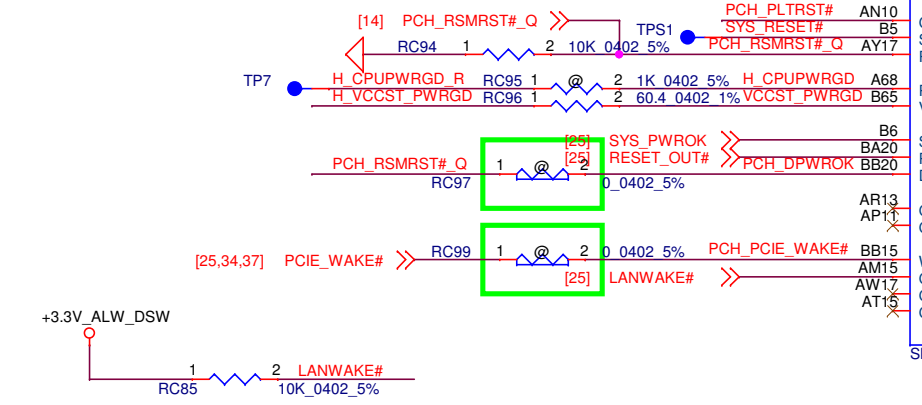
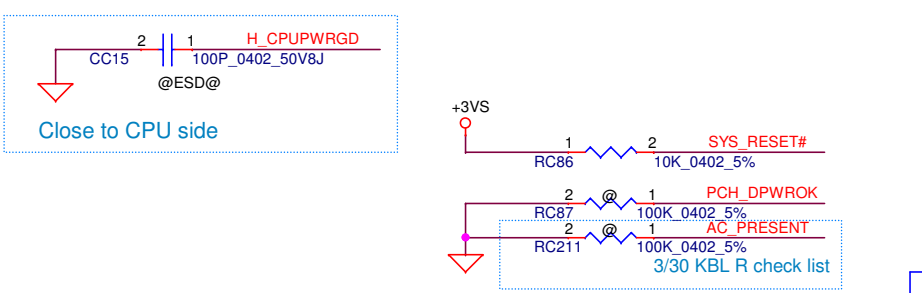
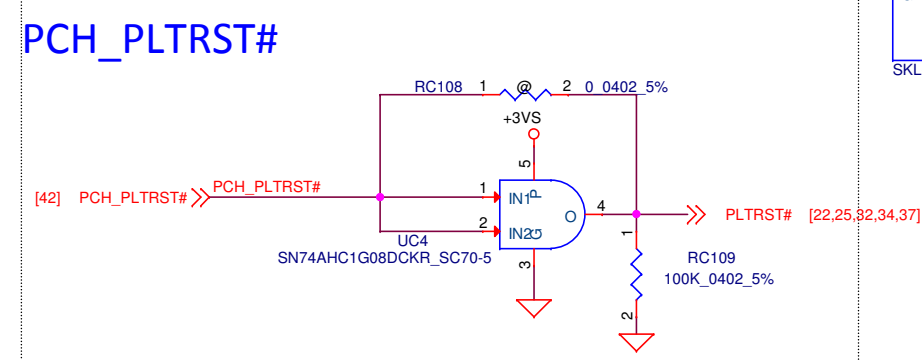
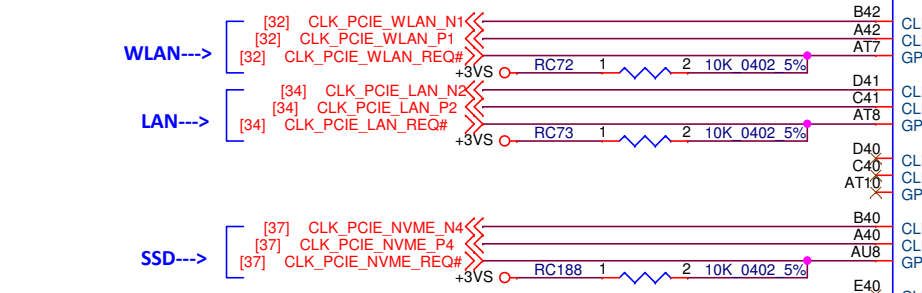


COMPENSATION PD FOR USBCOMP  
CAD Note:  
Max trace length < 1000 mil



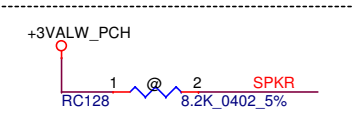
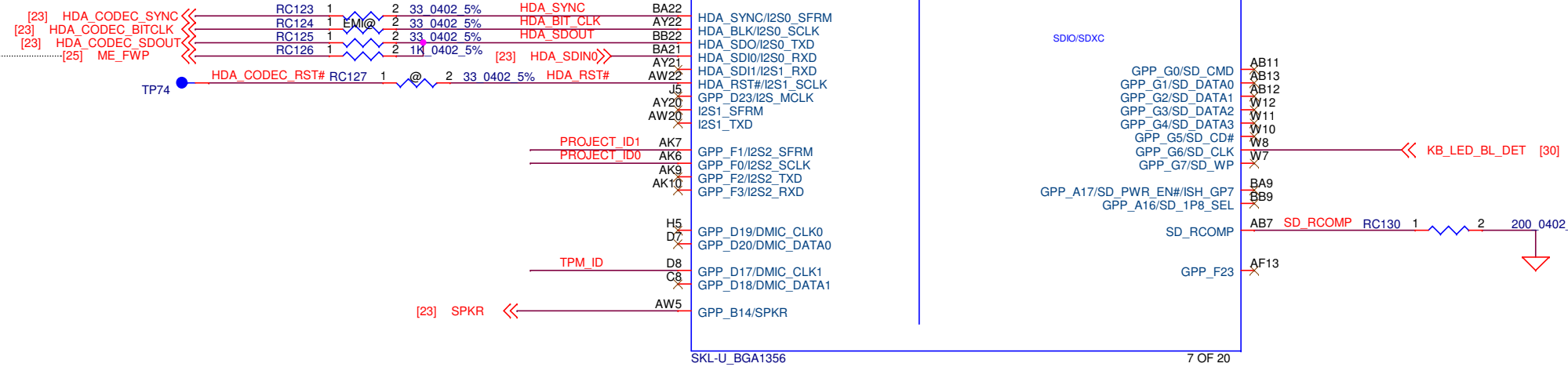
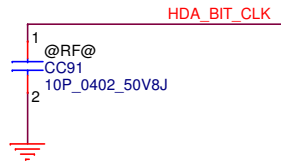
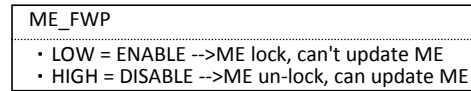
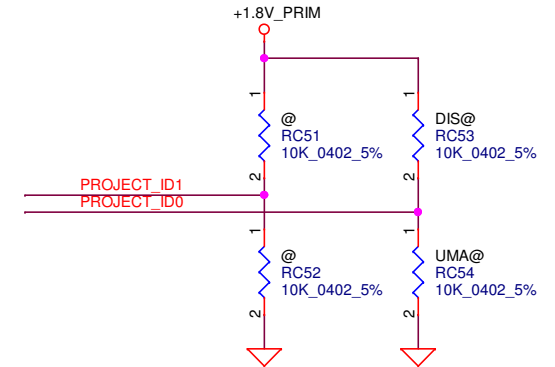
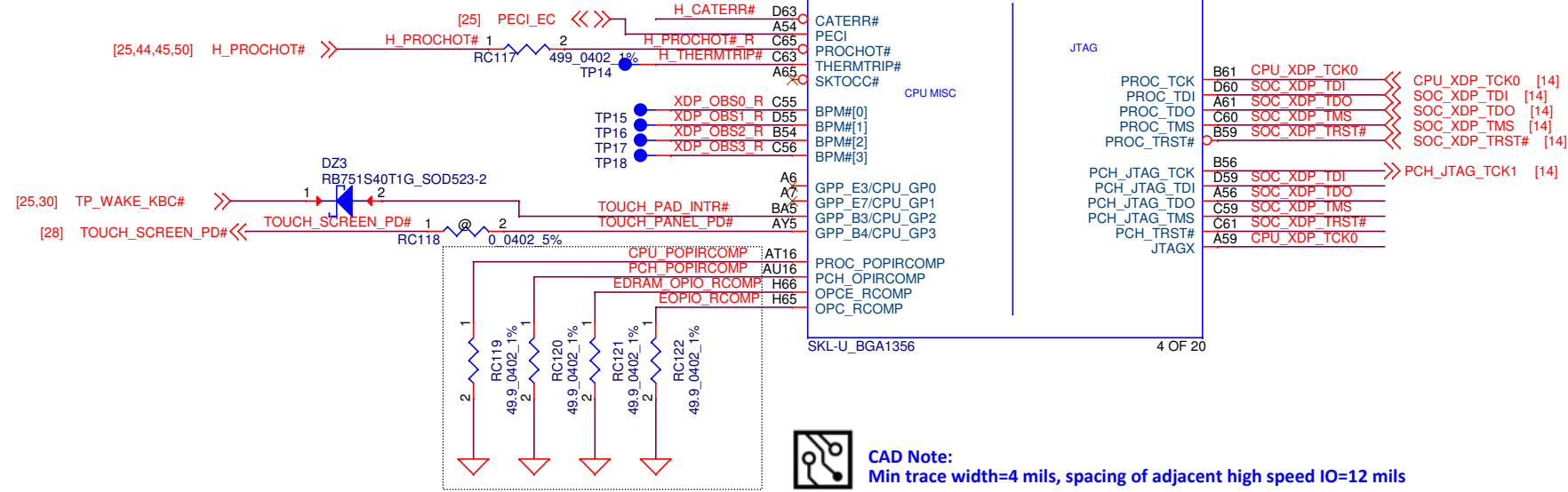
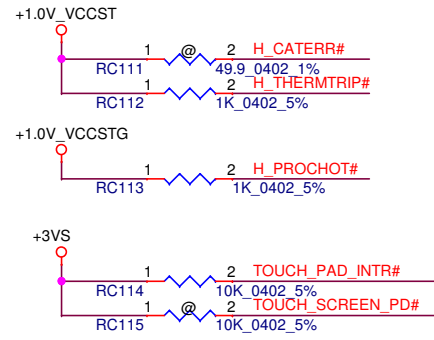
GPIO	Device Control
USB_OC0#	USB Port 1&Port3
USB_OC1#	USB Port 6
USB_OC2#	NA
USB_OC3#	NA

# Main Func = CPU

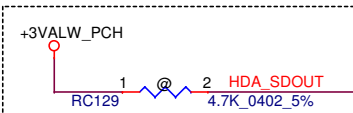


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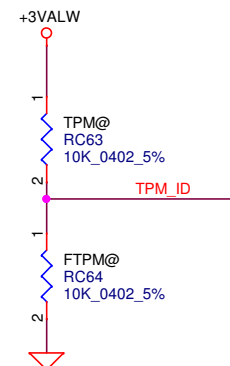
## Main Func = CPU



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

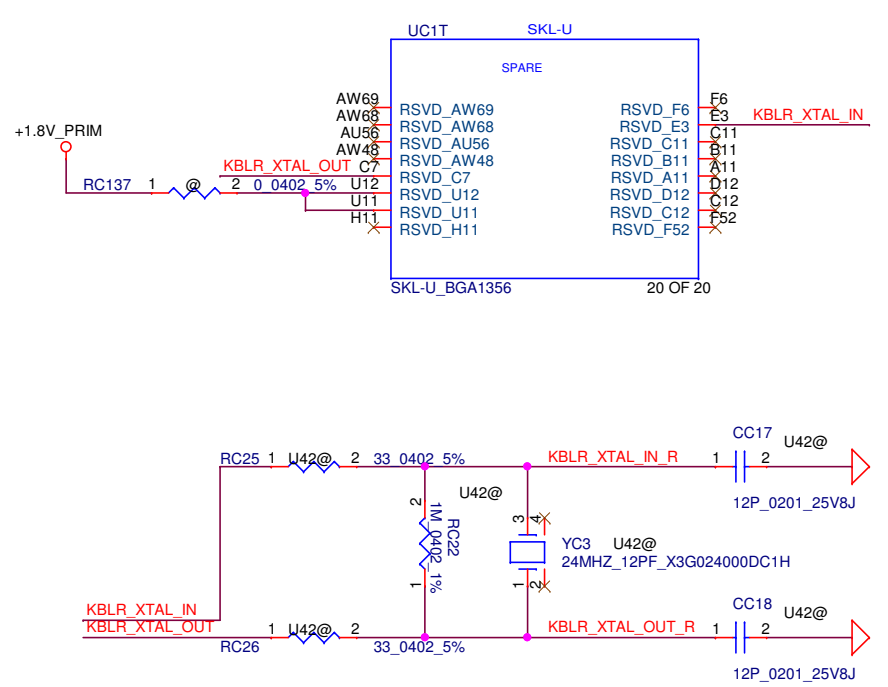
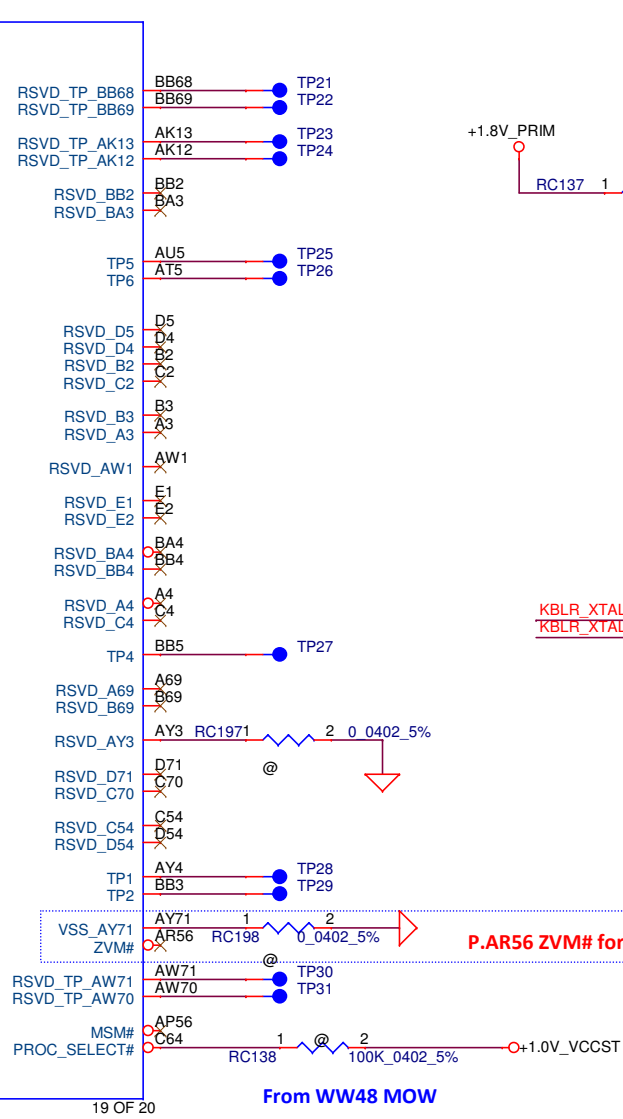
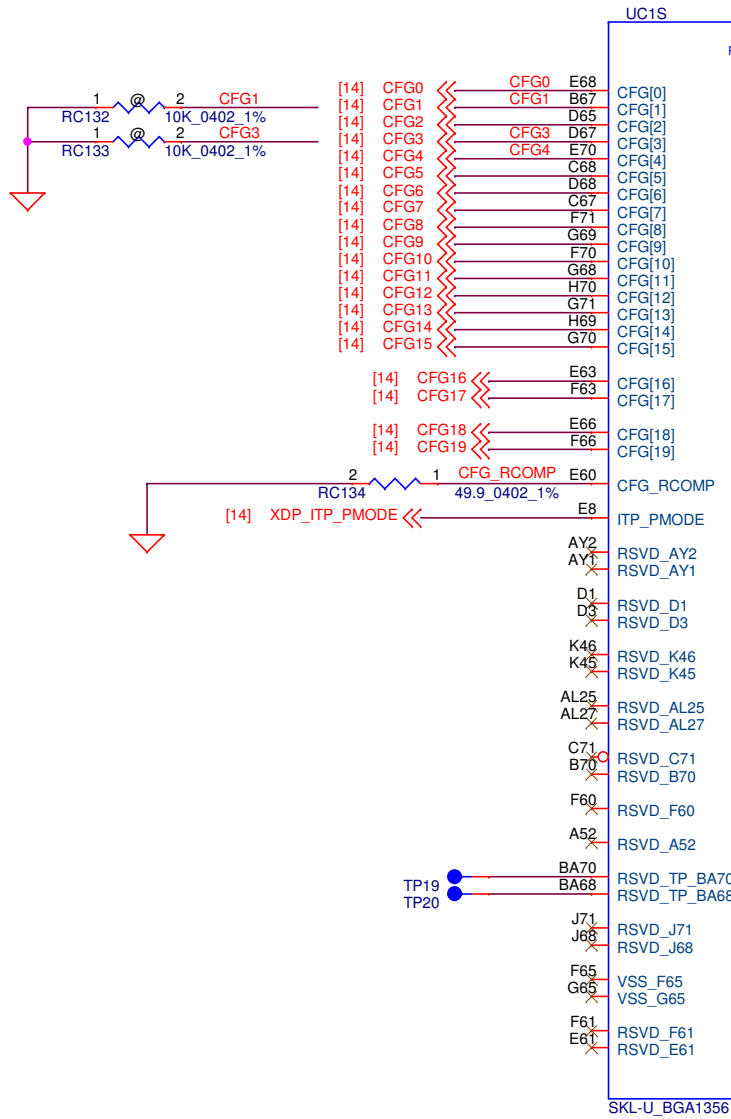
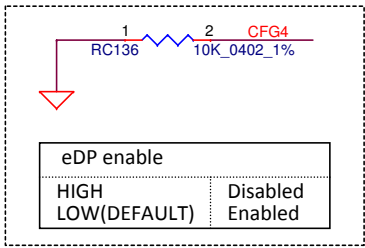
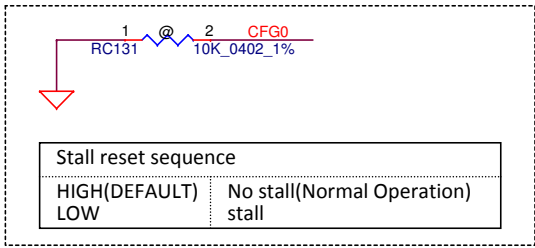


Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE



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					<b>LA-F114P</b>	A00
				Date:	Wednesday, July 26, 2017	Sheet 12 of 54

Main Func = CPU

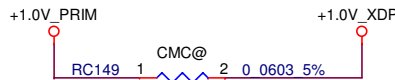
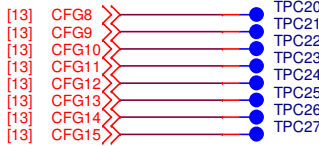
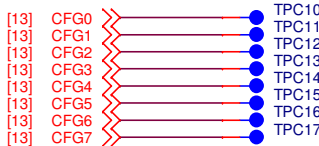
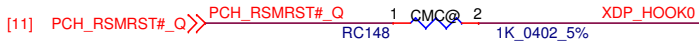


Connector Less Routing Topology

DCI Link  
RC142 need POP  
RC146 need POP

Place to CPU side

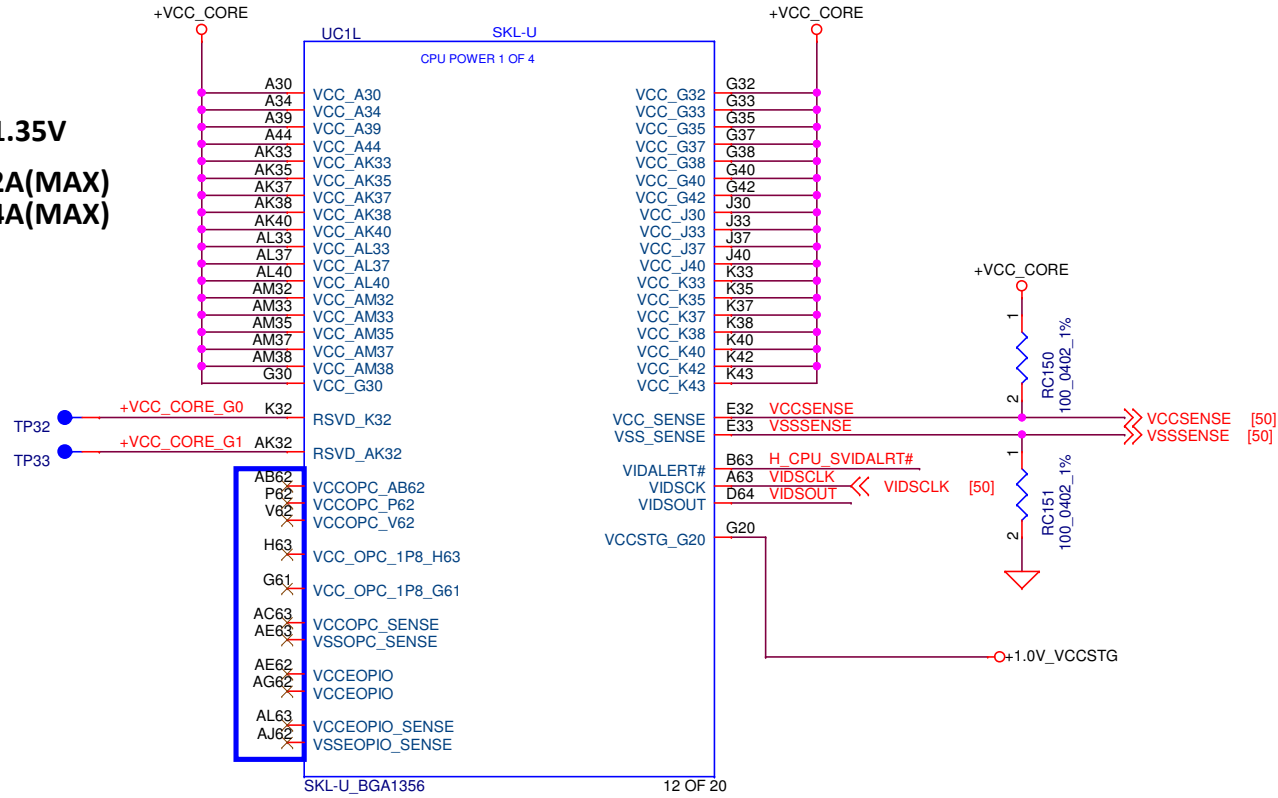
Place to CPU side



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		LA-F114P			A00
Date:		Wednesday, July 26, 2017		Sheet	14 of 54

Main Func = CPU

+VCC\_CORE: 0.3~1.35V  
+VCC\_CORE(U22): 32A(MAX)  
+VCC\_CORE(U42): 64A(MAX)

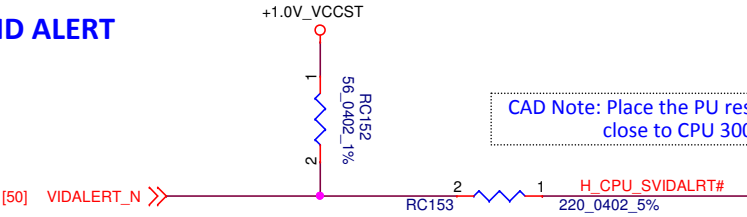


VCCOPC,VCCOPC\_1P8,VCCEOPIO for SKYLAKE-U 2+3e  
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

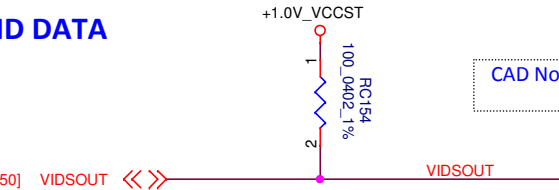
Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

SVID ALERT



CAD Note: Place the PU resistors close to CPU  
close to CPU 300 - 1500mils

SVID DATA



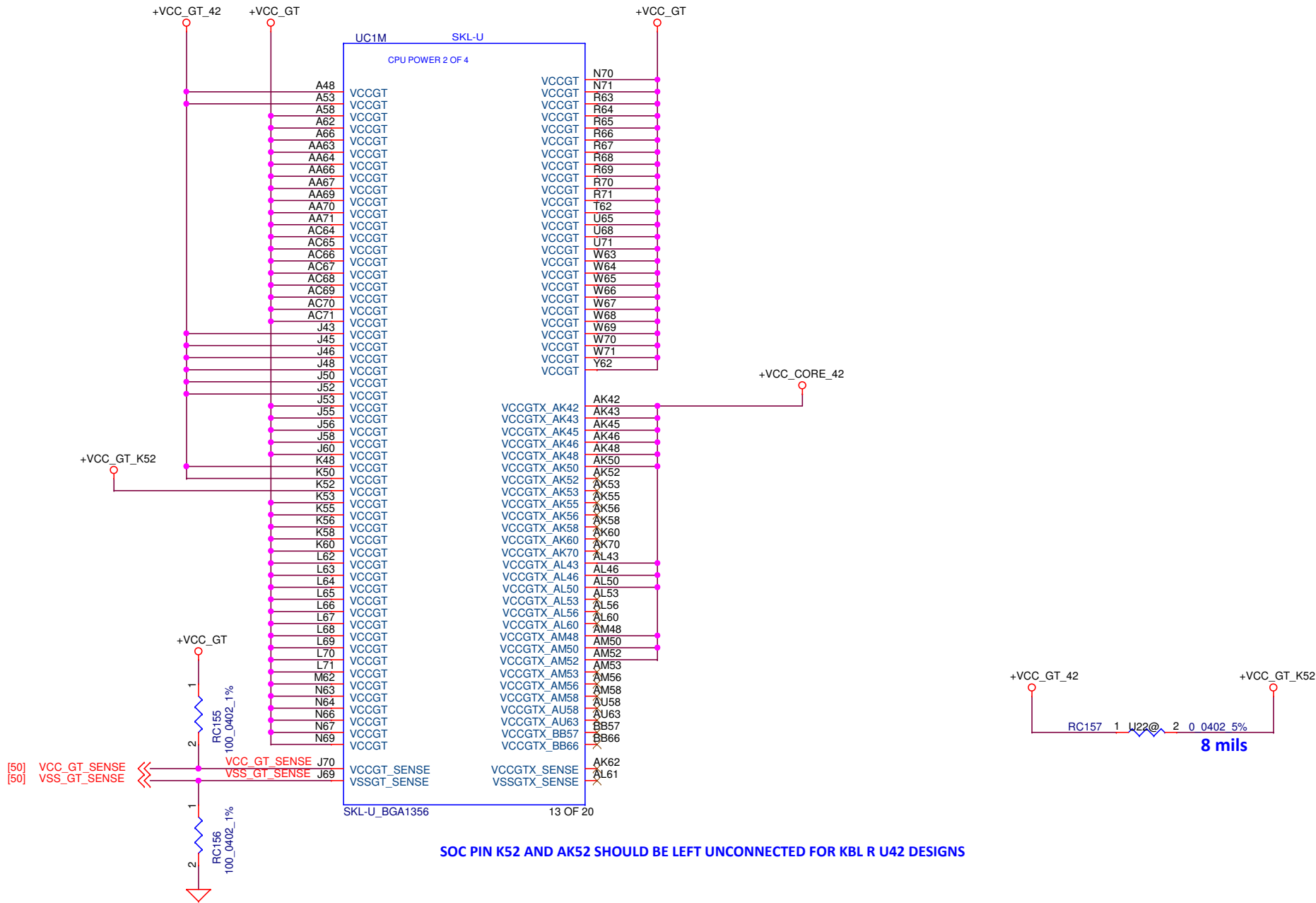
CAD Note: Place the PU resistors close to CPU  
close to CPU 300 - 1500mils

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Date: Wednesday, July 26, 2017		Sheet 15 of 54			

Main Func = CPU

+VCCGT: 0.3~1.35V  
+VCCGTX : 0.3~1.35V

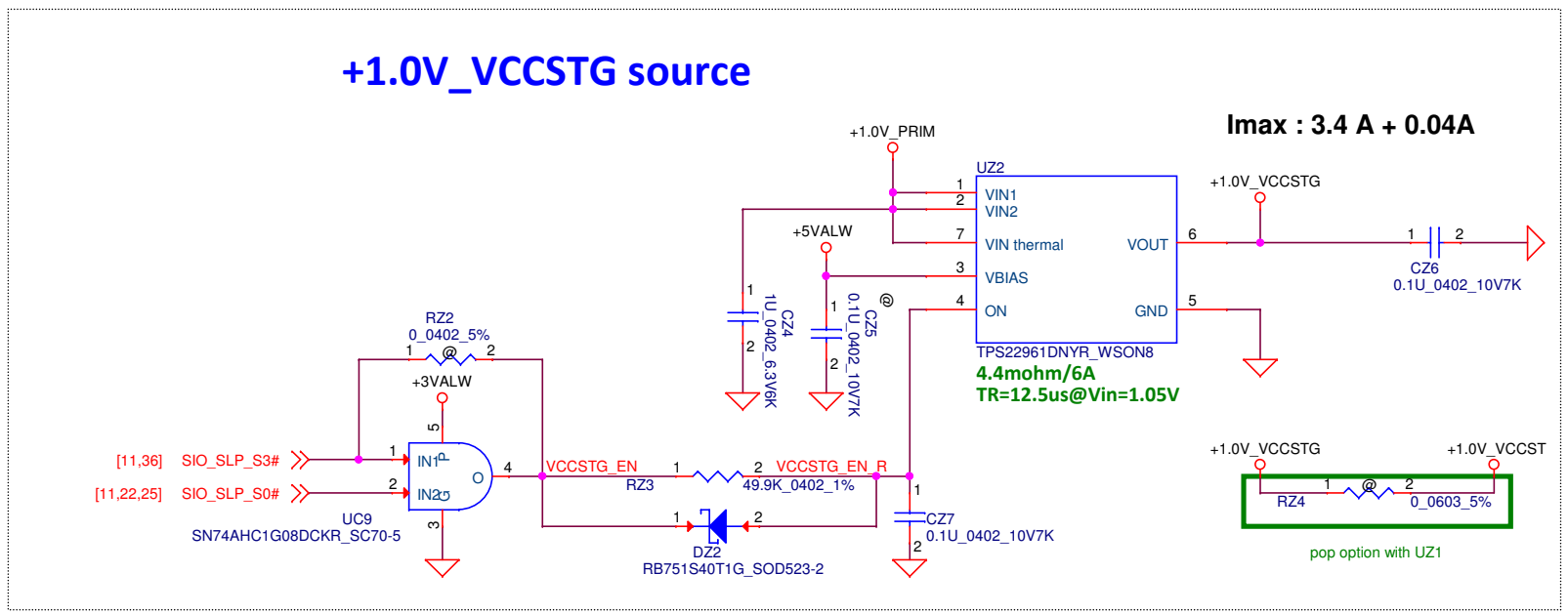
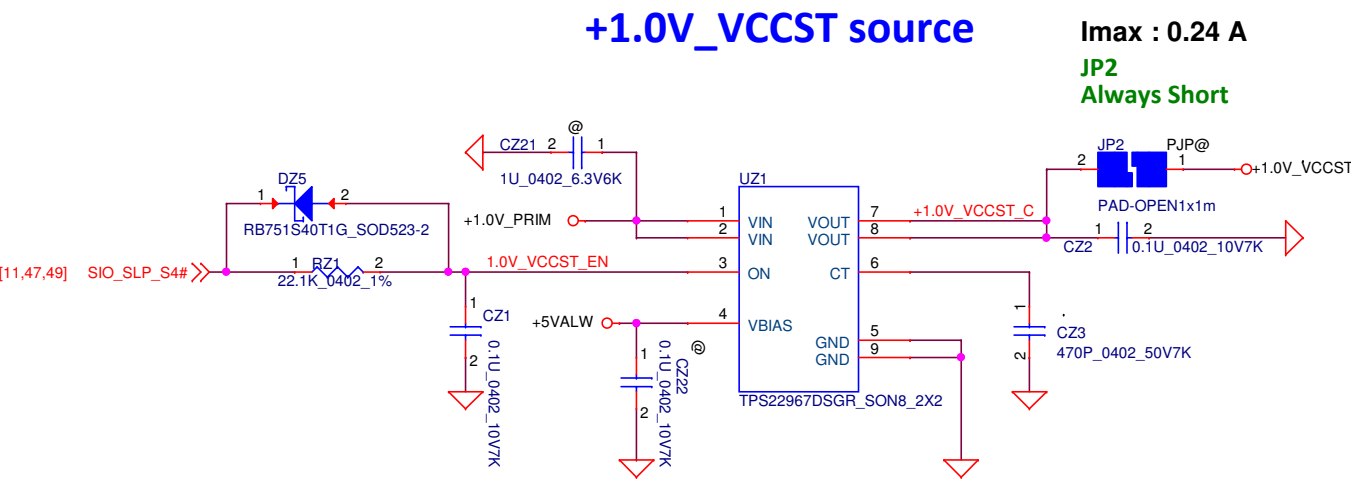
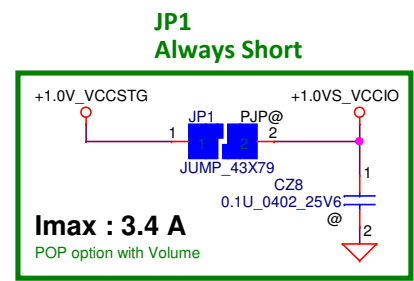
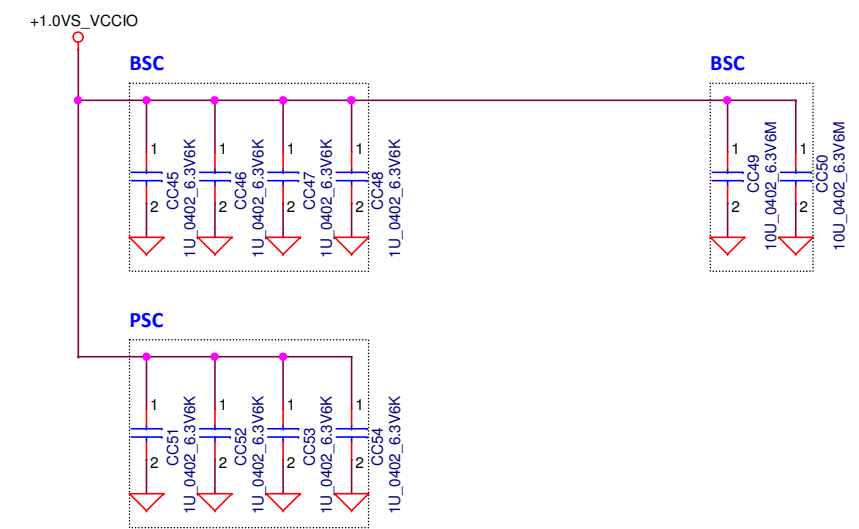
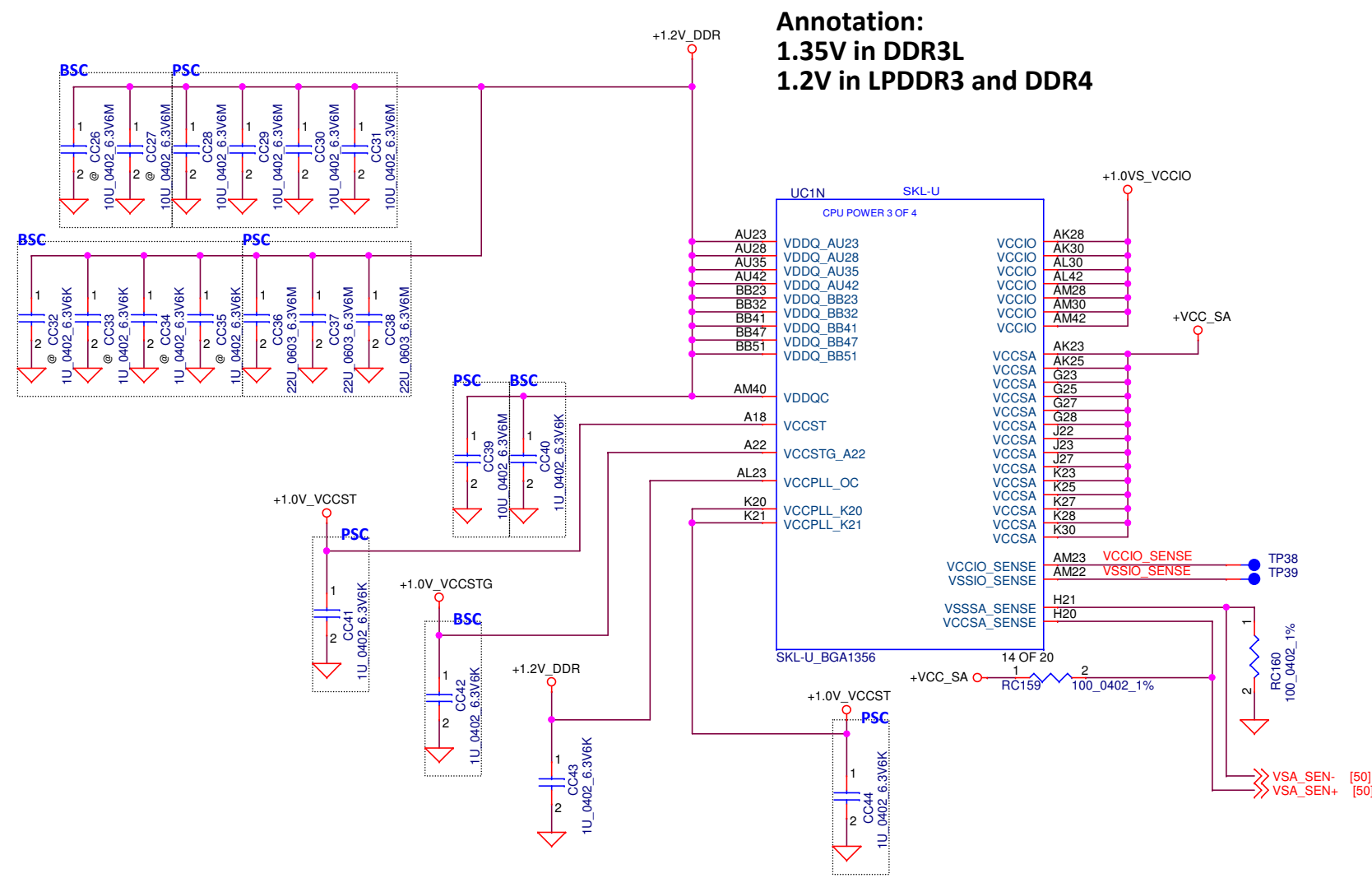
+VCC\_GT(U22): 31A(MAX)  
+VCC\_GT(U42): 28A(MAX)



SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

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		Custom		LA-F114P	Rev A00
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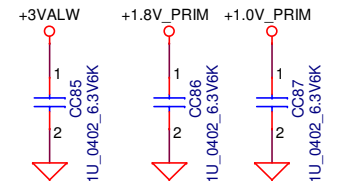
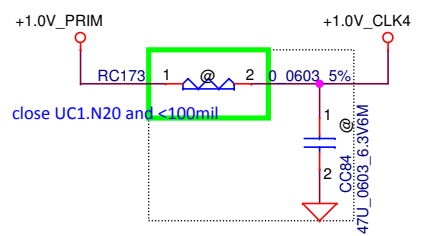
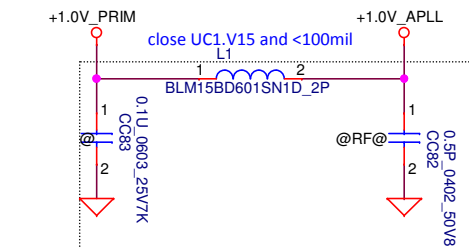
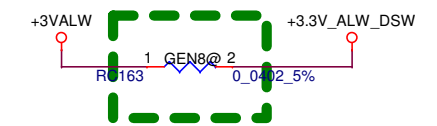
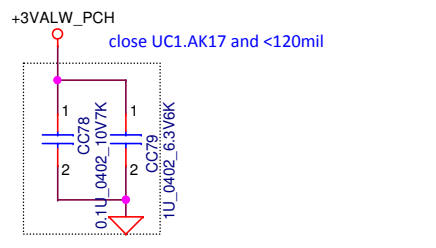
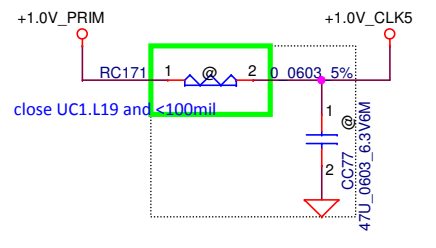
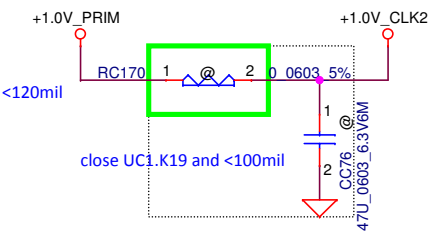
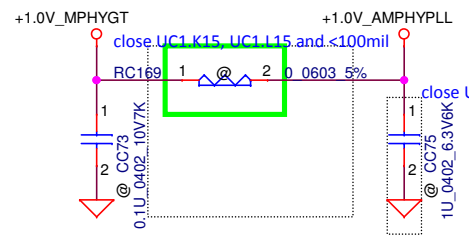
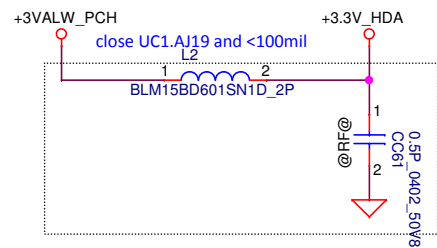
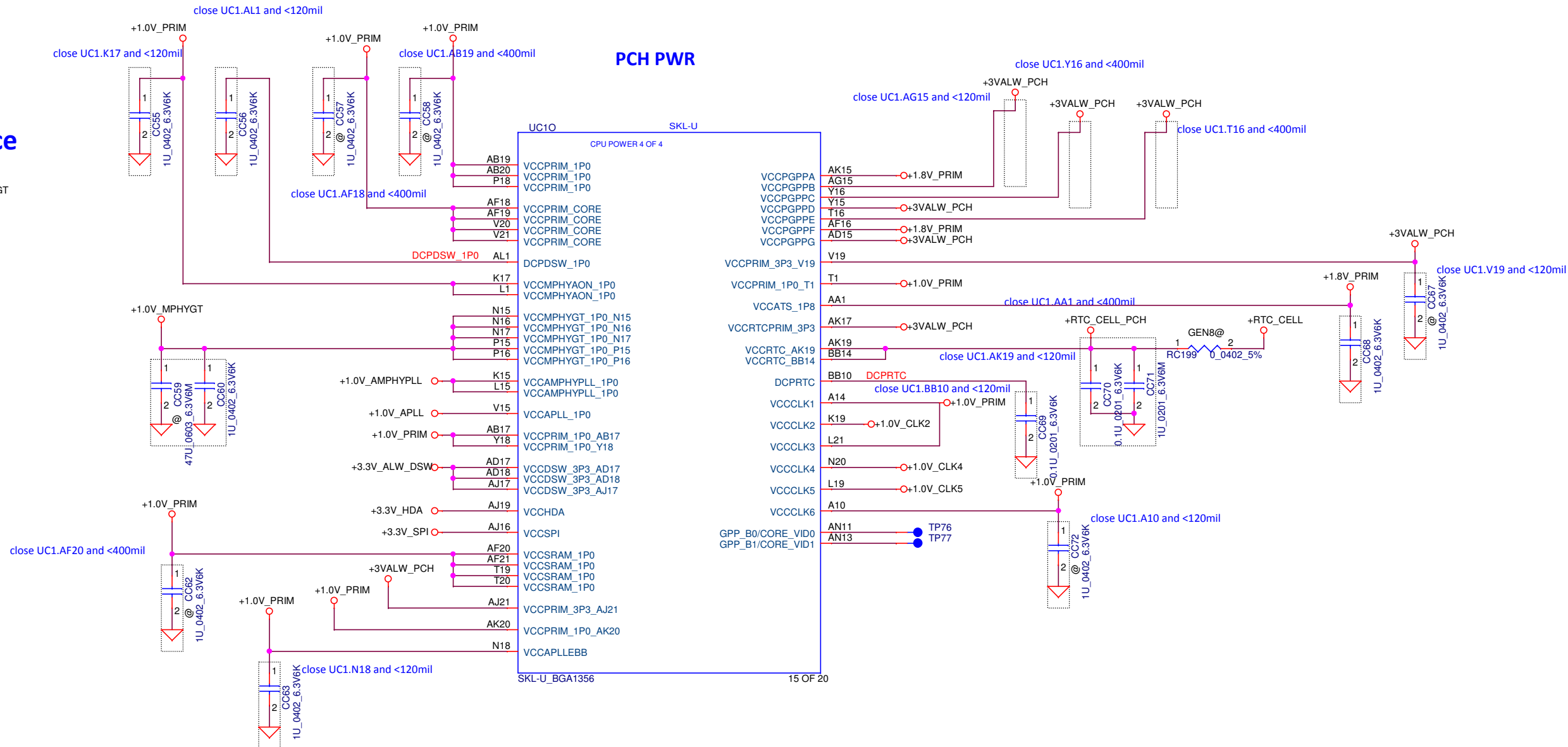
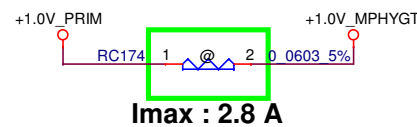
Main Func = CPU



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				Custom	LA-F114P
Date: Wednesday, July 26, 2017				Sheet	17 of 54

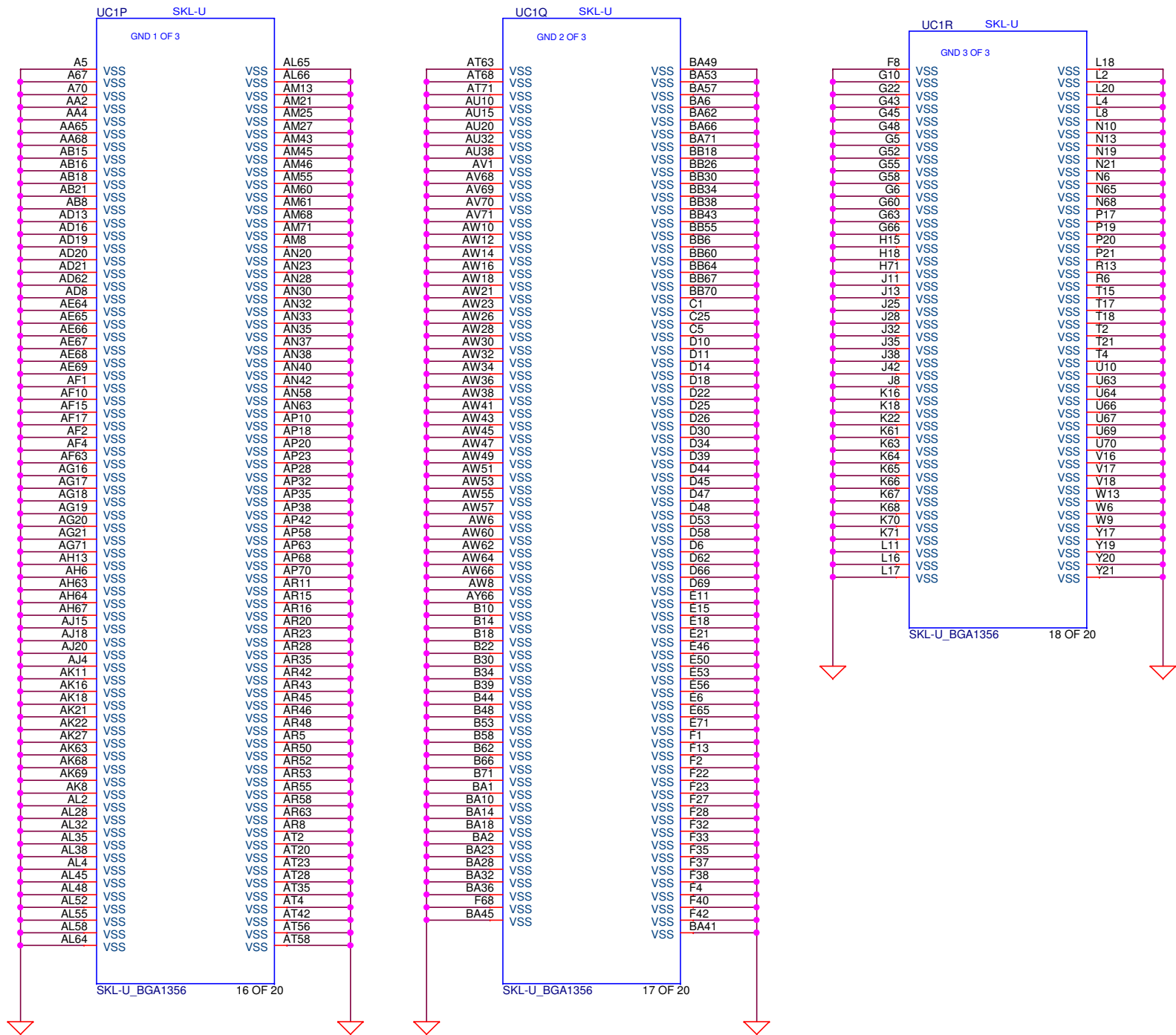
Main Func = CPU

+1.0V\_MPHYGT source



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Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE\_VID[1:0] to the VR and fix PCH VCCPRIM\_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM\_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE\_VID[1:0] to the VR.

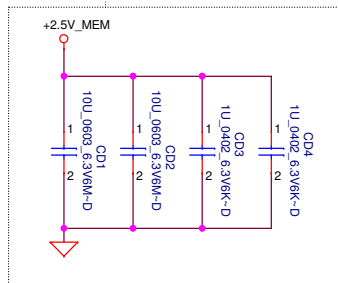
- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

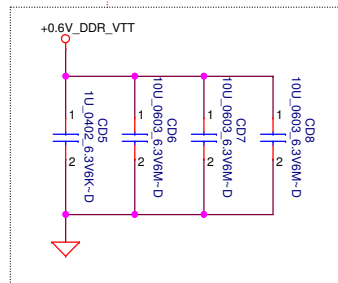
Security Classification		Compal Secret Data		Title	
Issued Date		2016/12/01	Deciphered Date	2017/12/01	Compal Electronics, Inc. <b>MCP(14/14)VSS</b>
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		LA-F114P		A00	
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## Main Func = DDR

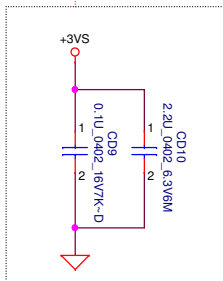
Layout Note:  
Place near JDIMM1.257,259



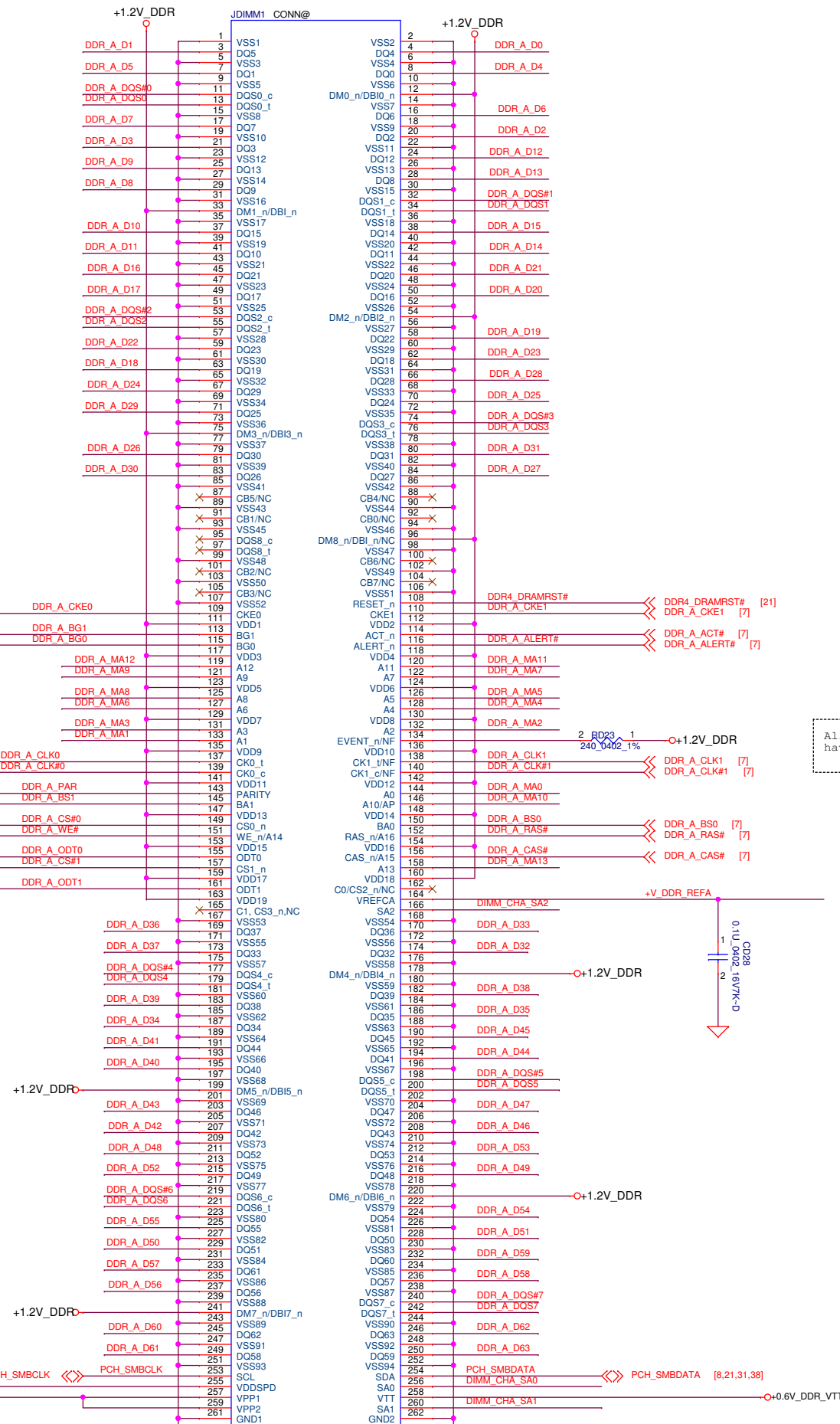
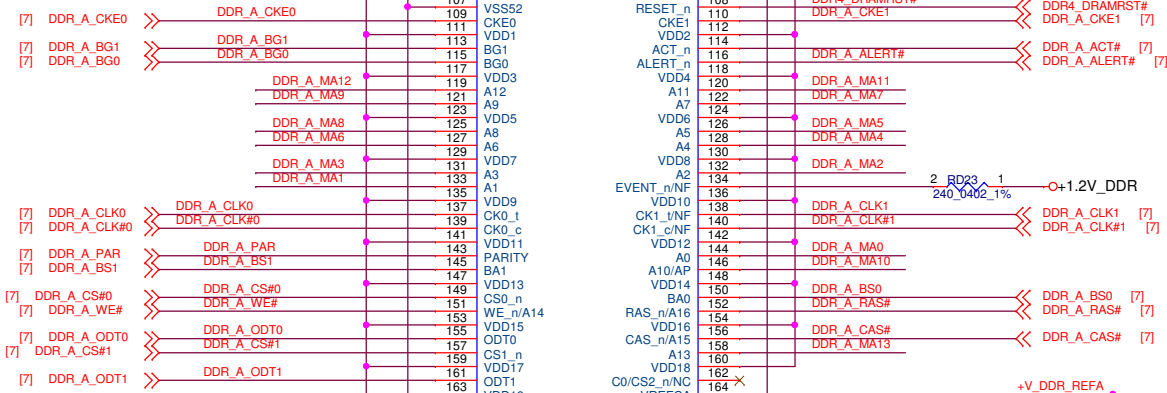
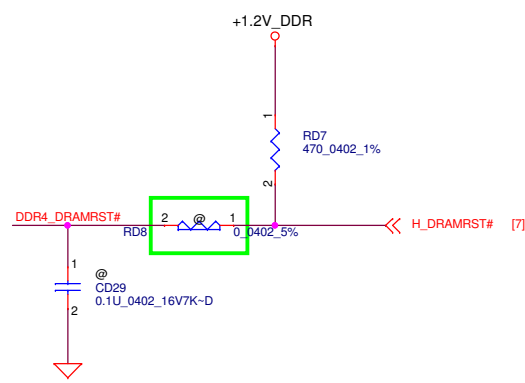
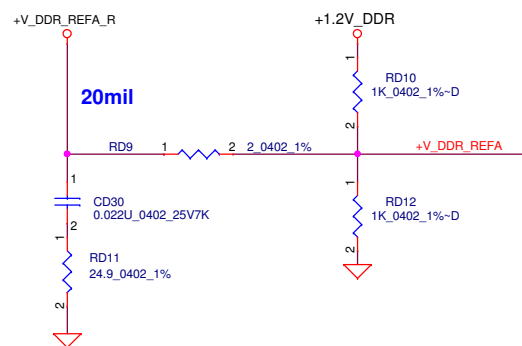
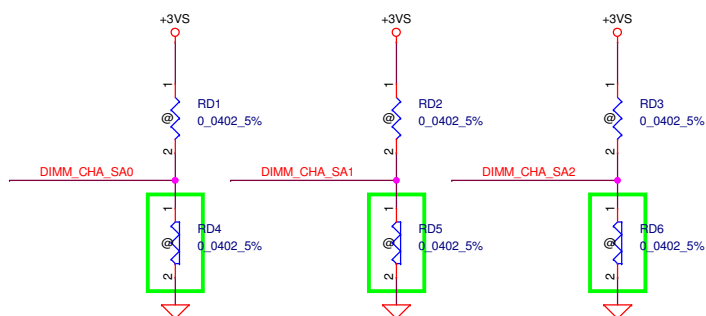
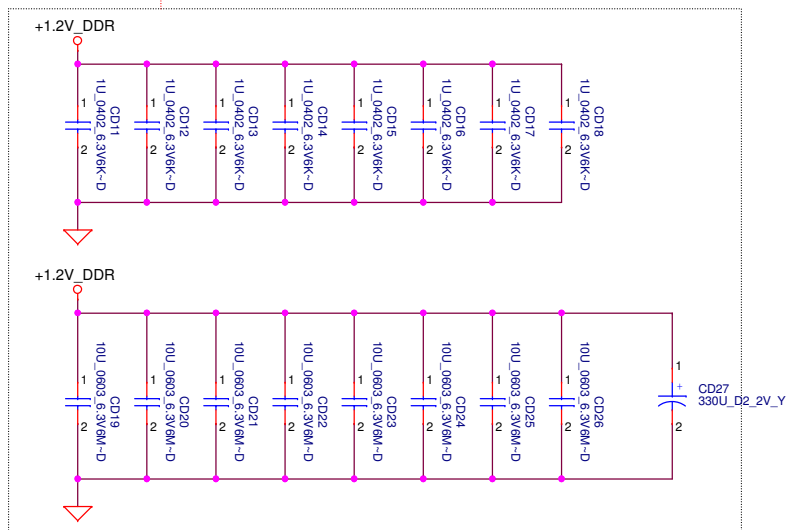
Layout Note:  
Place near JDIMM1.258



Layout Note:  
Place near JDIMM1.255



Layout Note:  
Place near JDIMM1

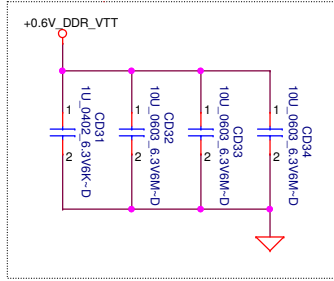


All VREF traces should have 10 mil trace width

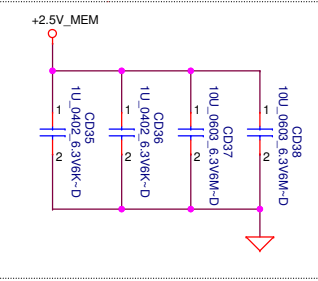
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>DDR4 DIMMA RVS</b>	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	
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Main Func = DDR

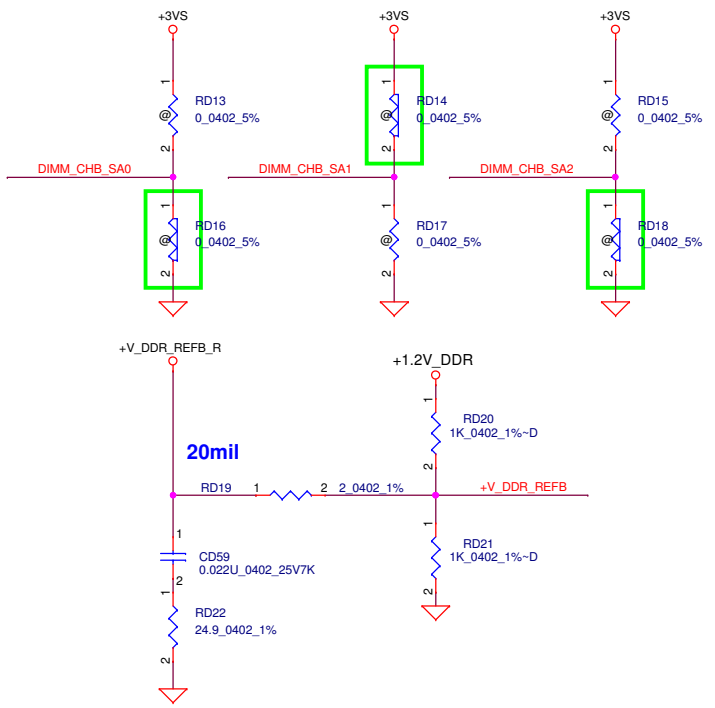
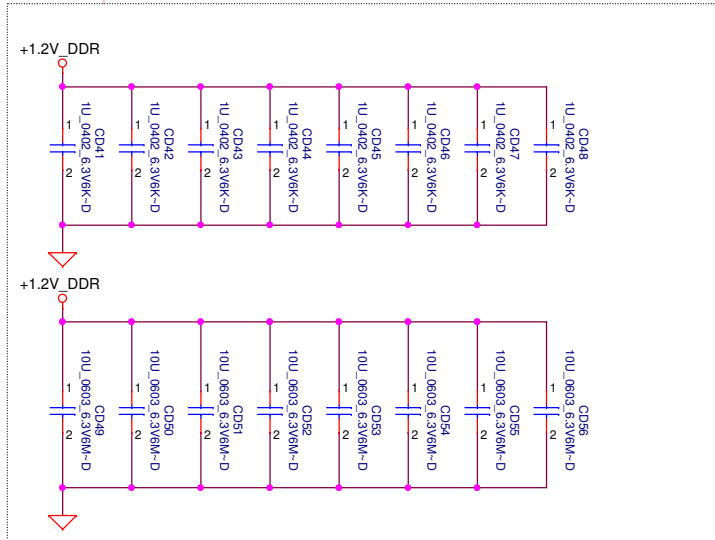
Layout Note:  
Place near JDIMM2.258



Layout Note:  
Place near JDIMM2.257,259

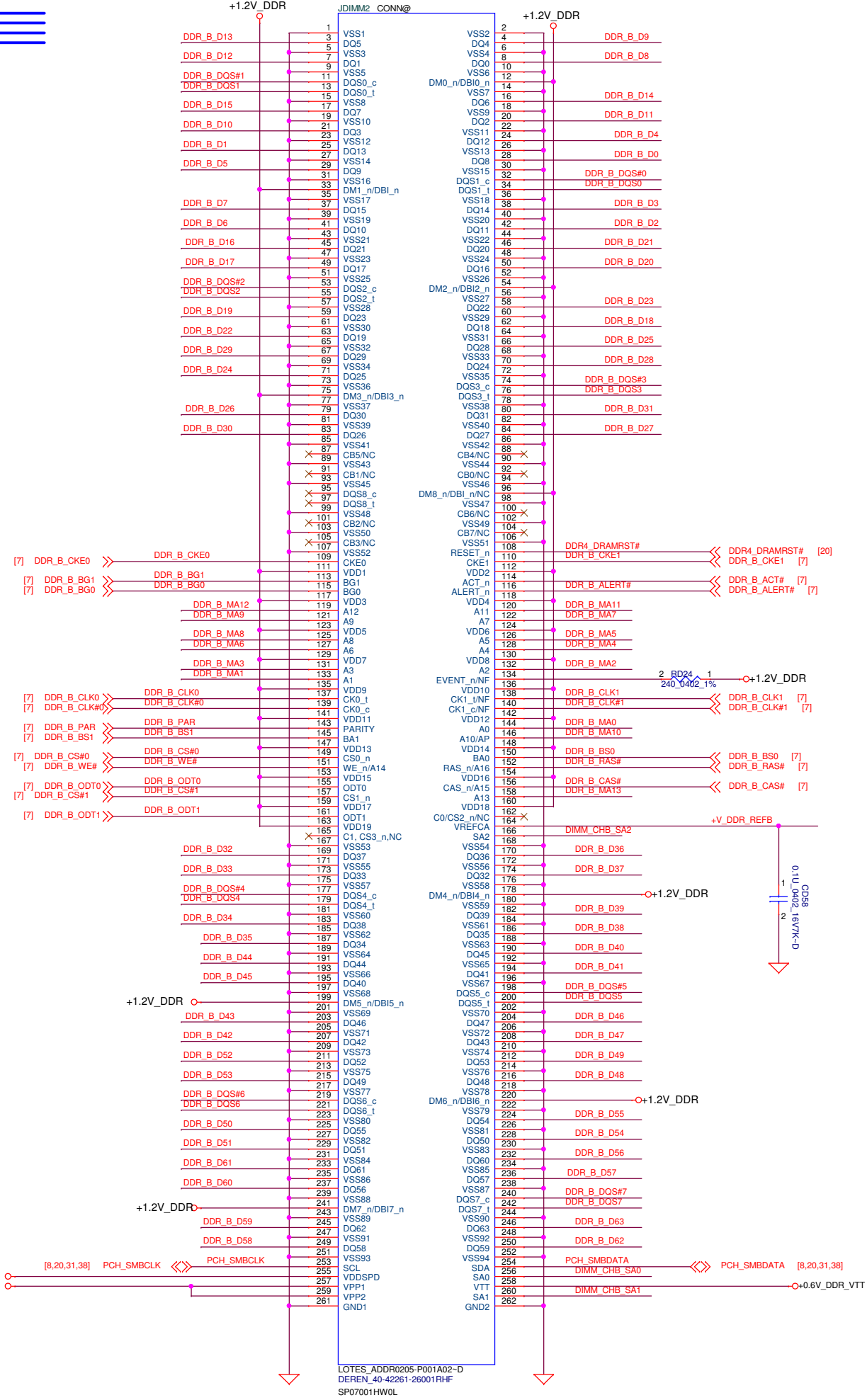
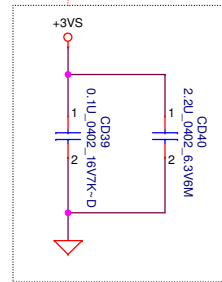


Layout Note:  
Place near JDIMM2



[7] DDR\_B\_D[0..63]  
[7] DDR\_B\_MA[0..13]  
[7] DDR\_B\_DQS#[0..7]  
[7] DDR\_B\_DQS[0..7]

Layout Note:  
Place near JDIMM2.255

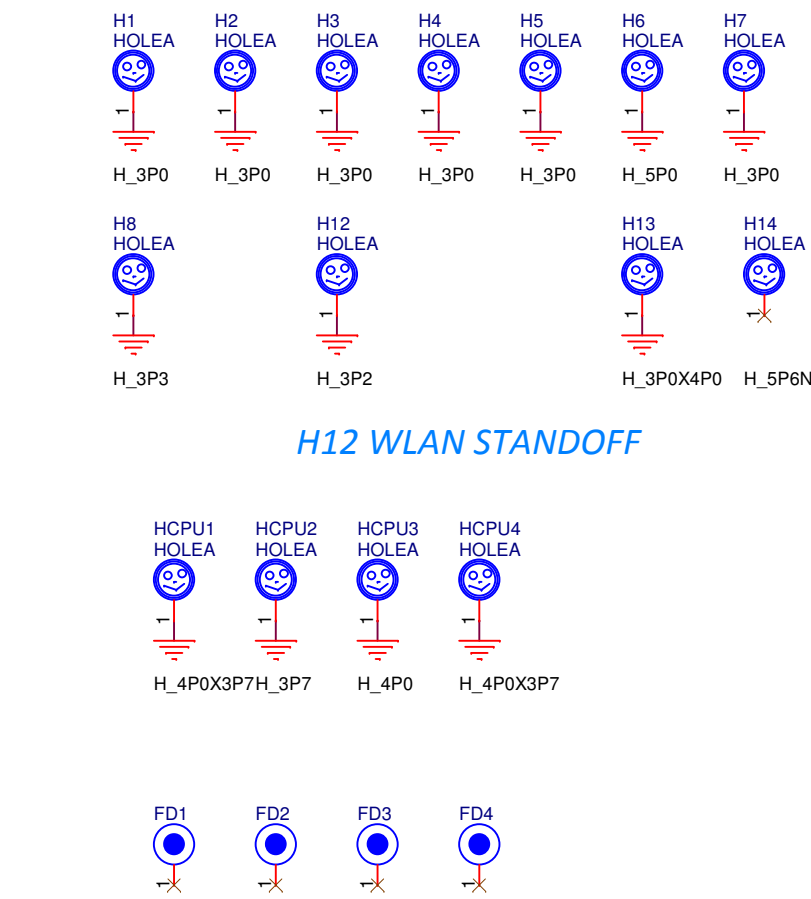


All VREF traces should  
have 10 mil trace width

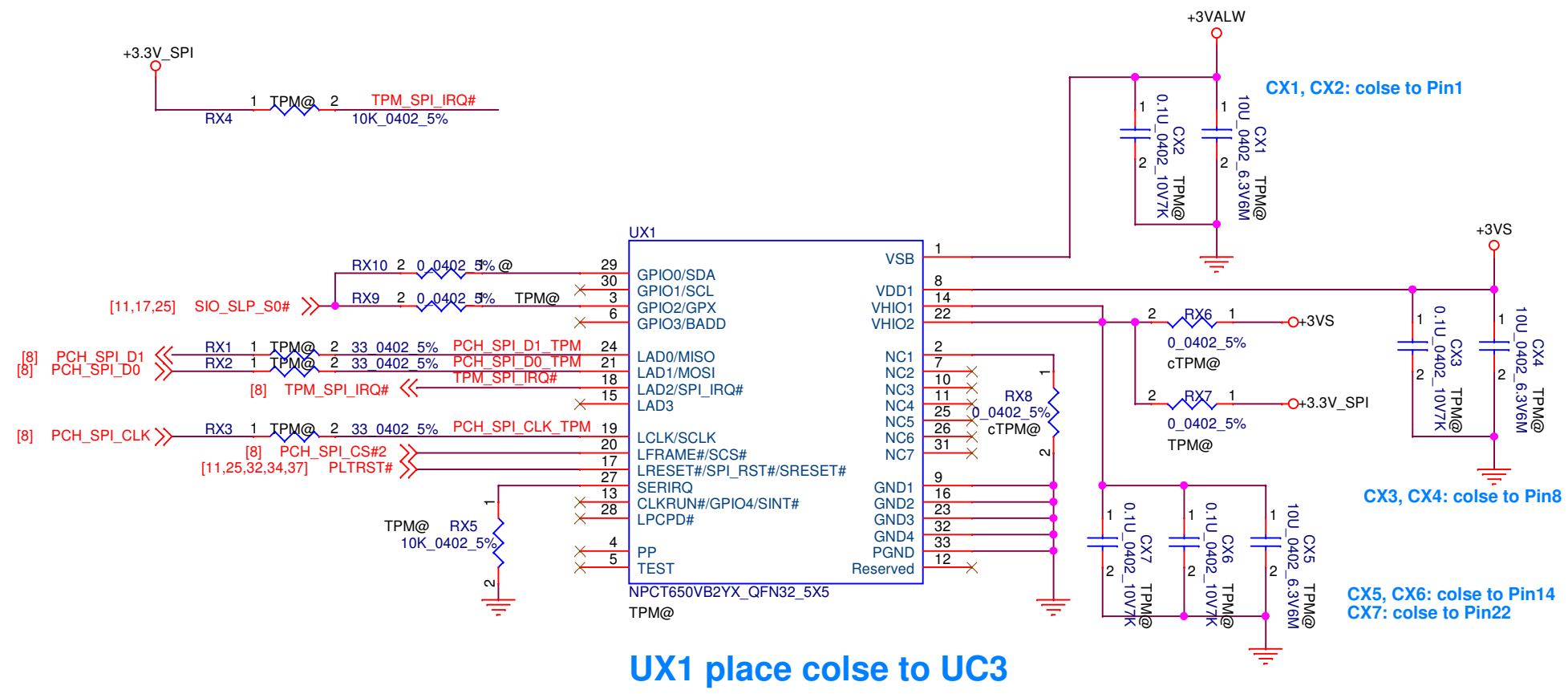
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Main Func = TPM

Screw hole/FD



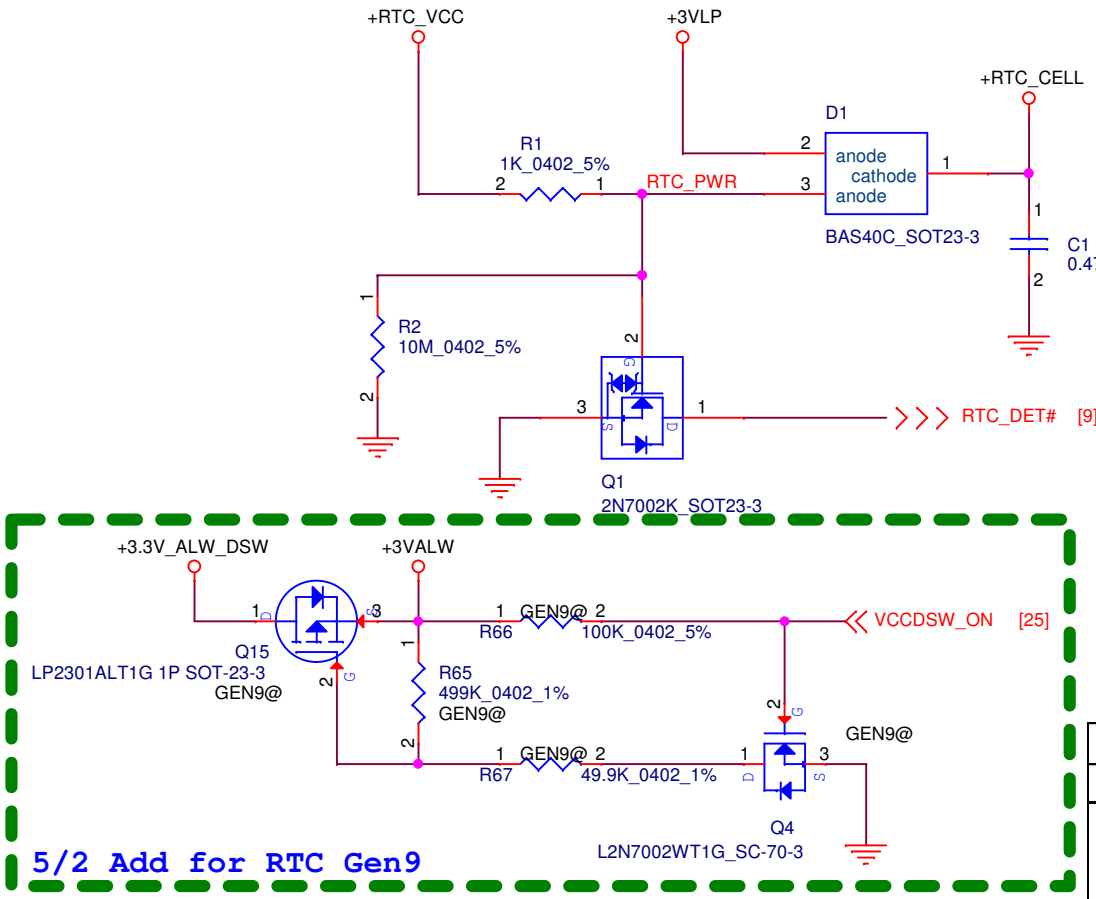
H12 WLAN STANDOFF



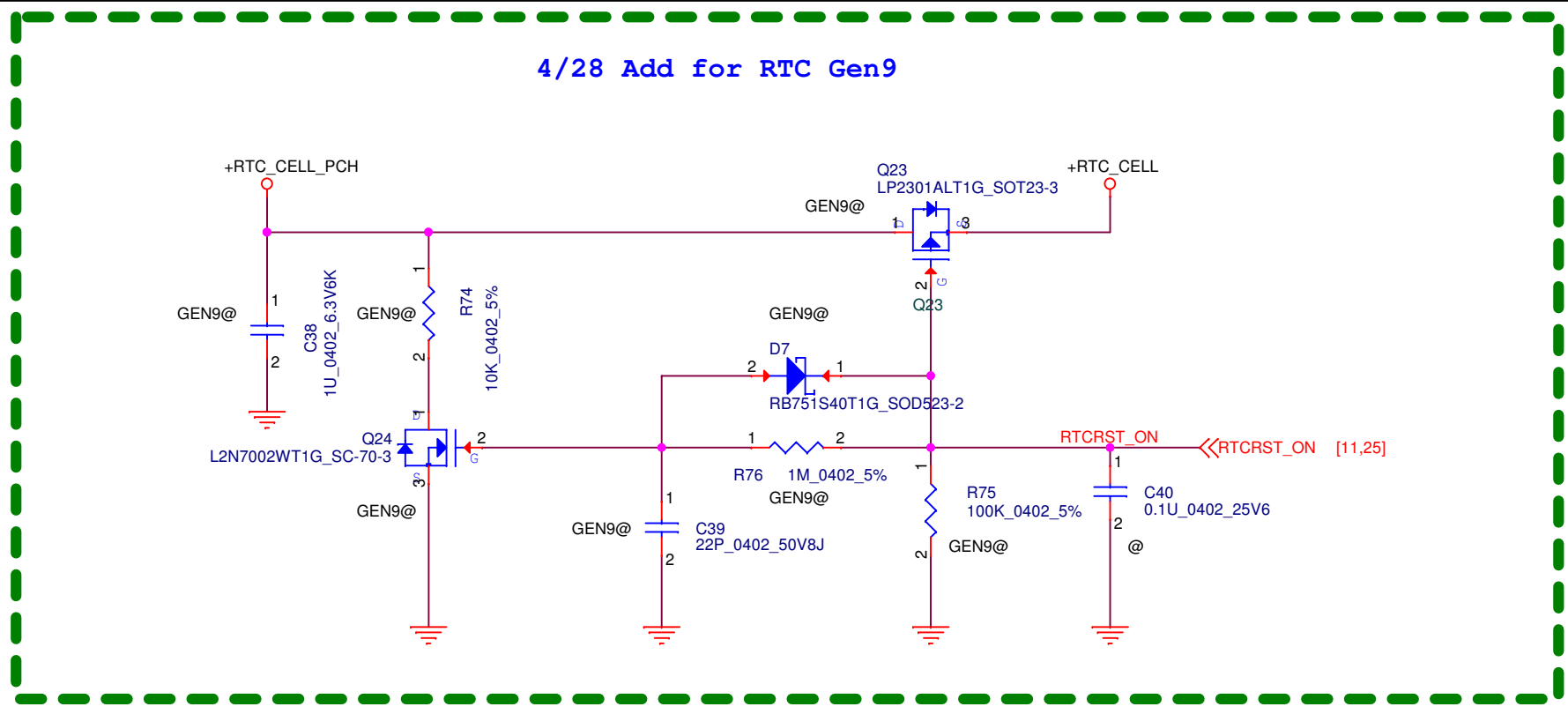
UX1 place colse to UC3

	Mounted	Unmounted	Comments
NPCT65x	RX5, RX7	RX6	VDD_VHIO - V_RUN Power VHIO - V_SPI Power
NPCT75x	RX6	RX5, RX7	VDD_VHIO and VHIO - V_RUN Power

Main Func = RTC

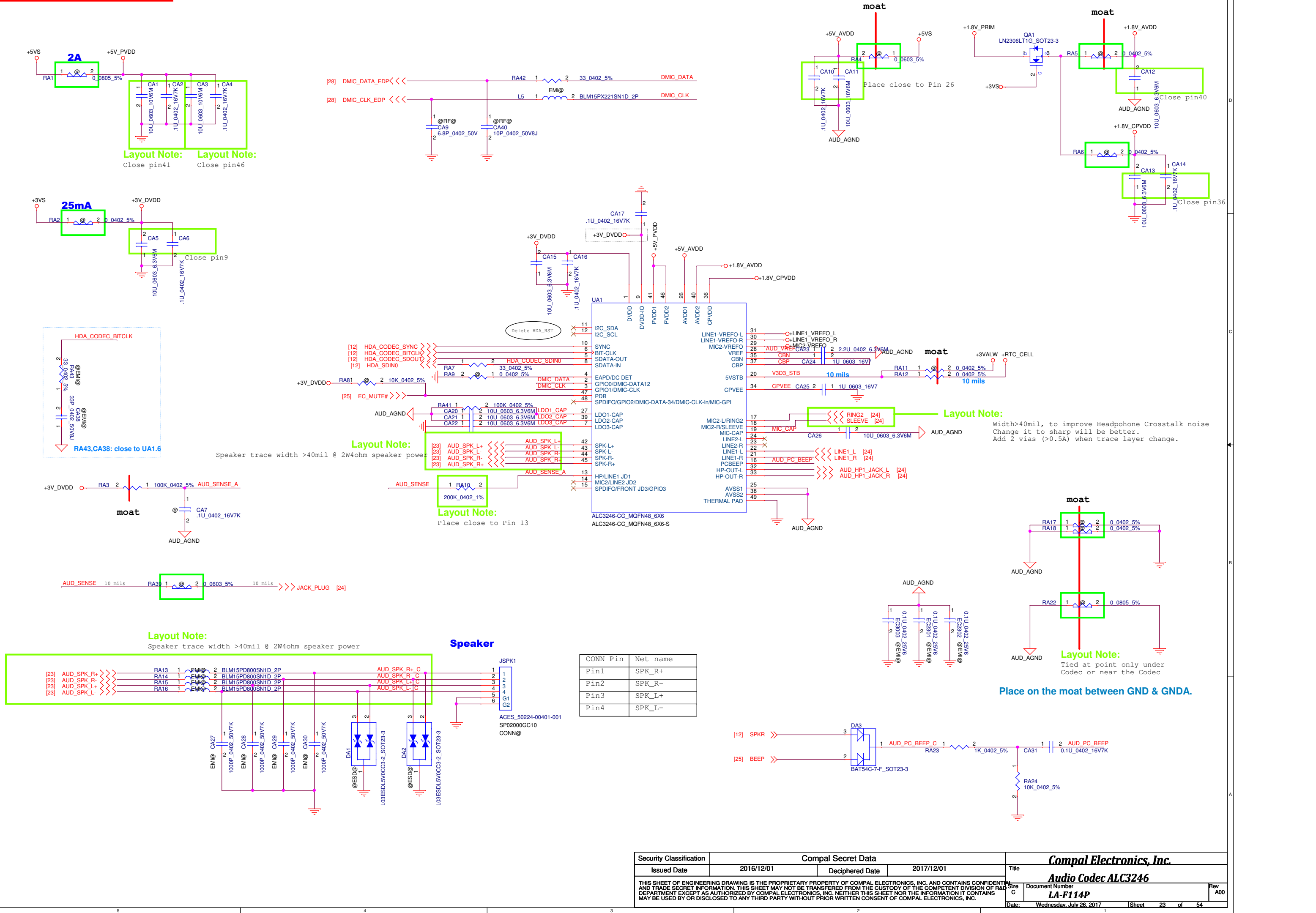


5/2 Add for RTC Gen9

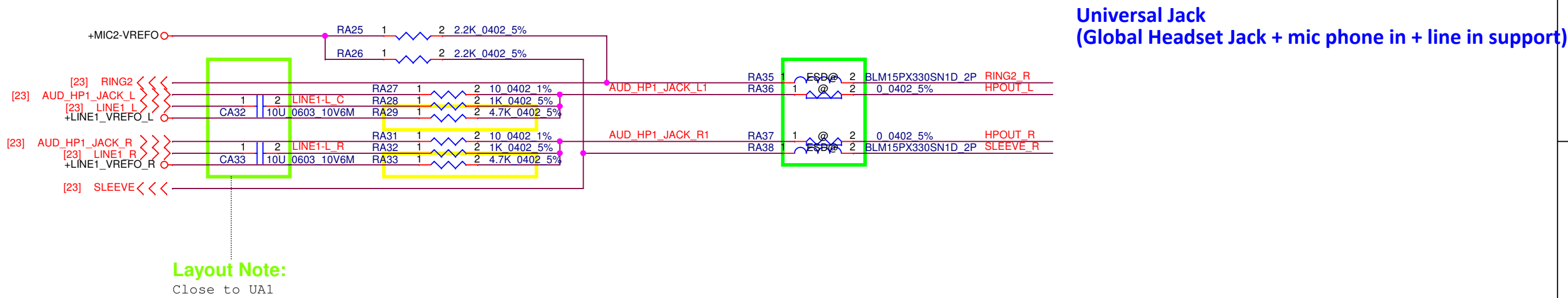


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Date: Wednesday, July 26, 2017				Sheet 22 of 54

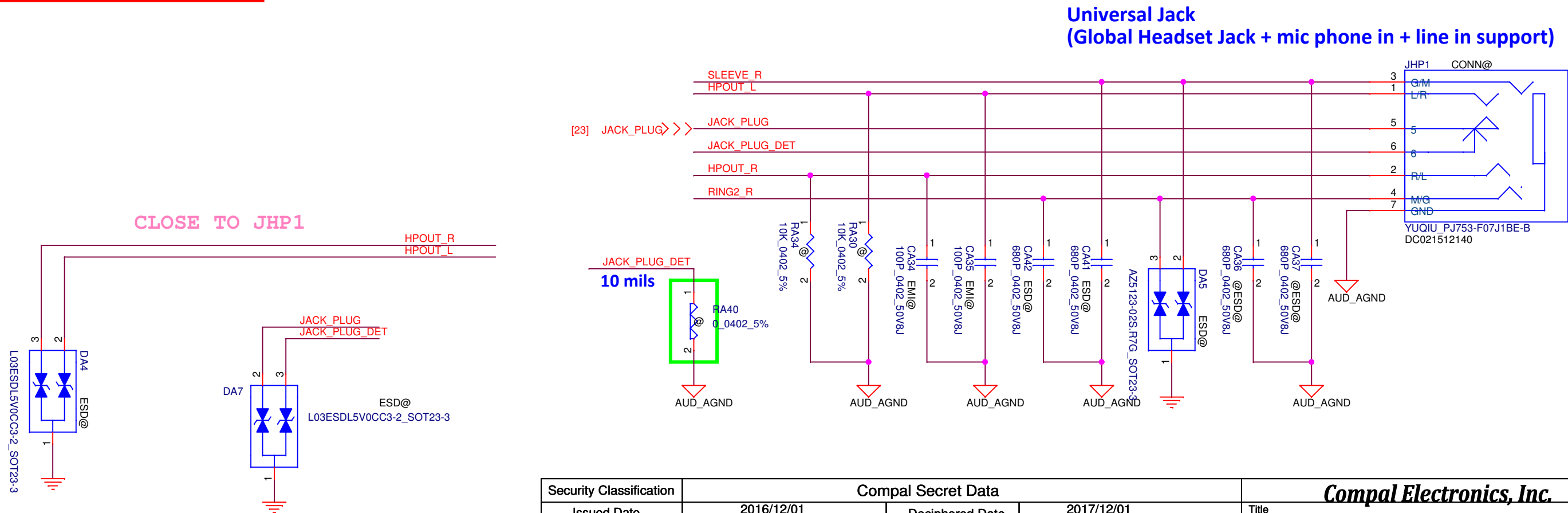
Main Func = Audio



Main Func = Audio Jack



Main Func = Audio Jack

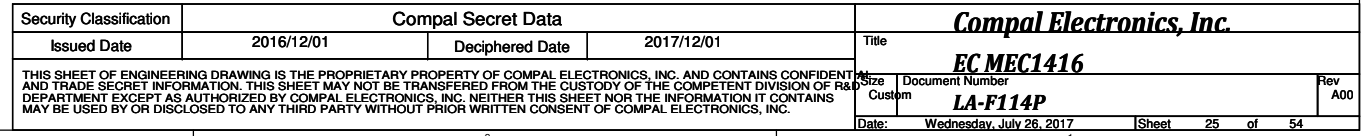
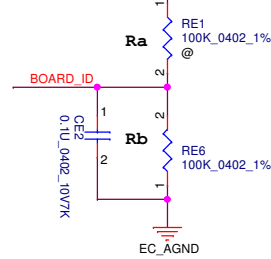
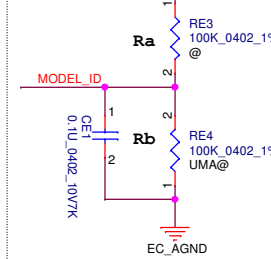


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Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title	Audio JACK
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				Document Number	LA-F114P
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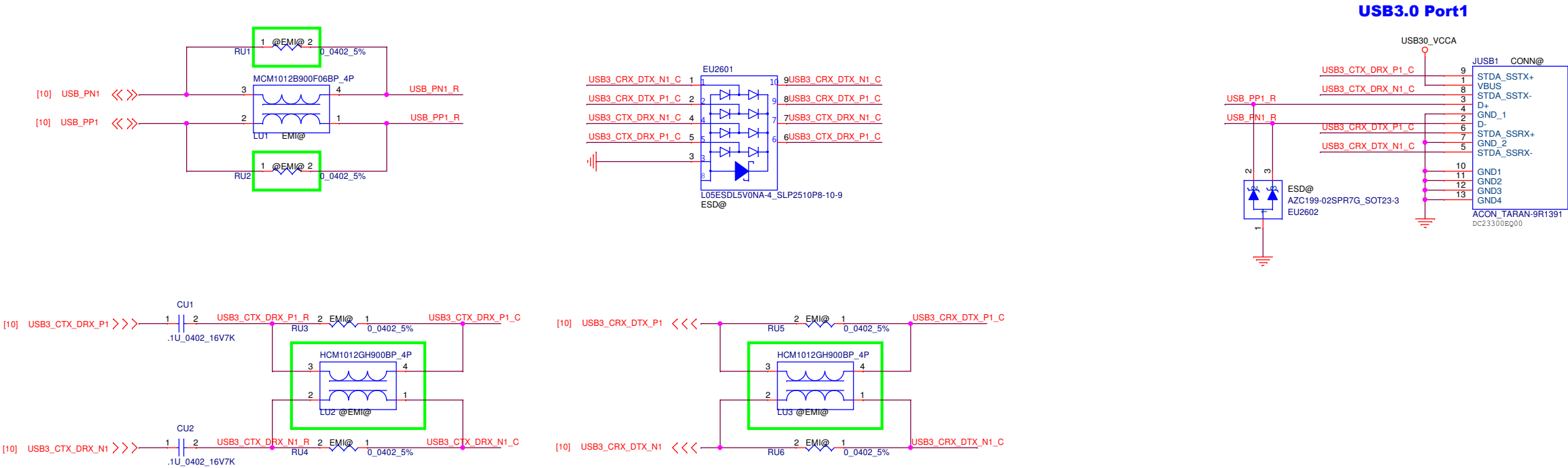
UE1 EC@  
EC Chip CPN  
MEC1416-NU-D0\_VTQFP128\_14X14  
SA0000A8L00

RE1 EC@  
49.9K\_0402\_1%  
SD034499280

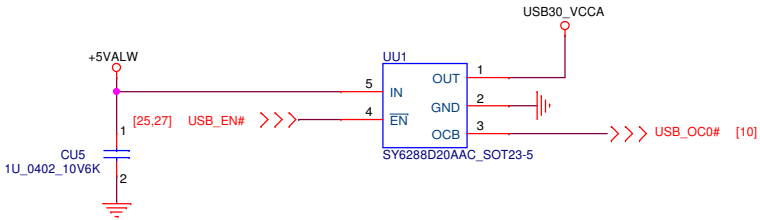
Board ID



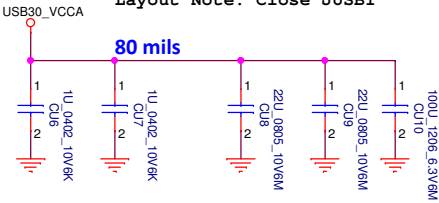
Main Func = USB3.0 Port1



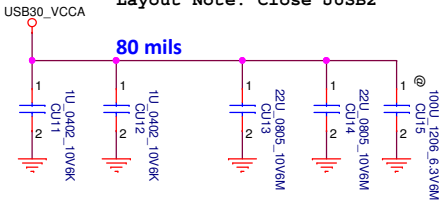
Maximum Output Current 2A



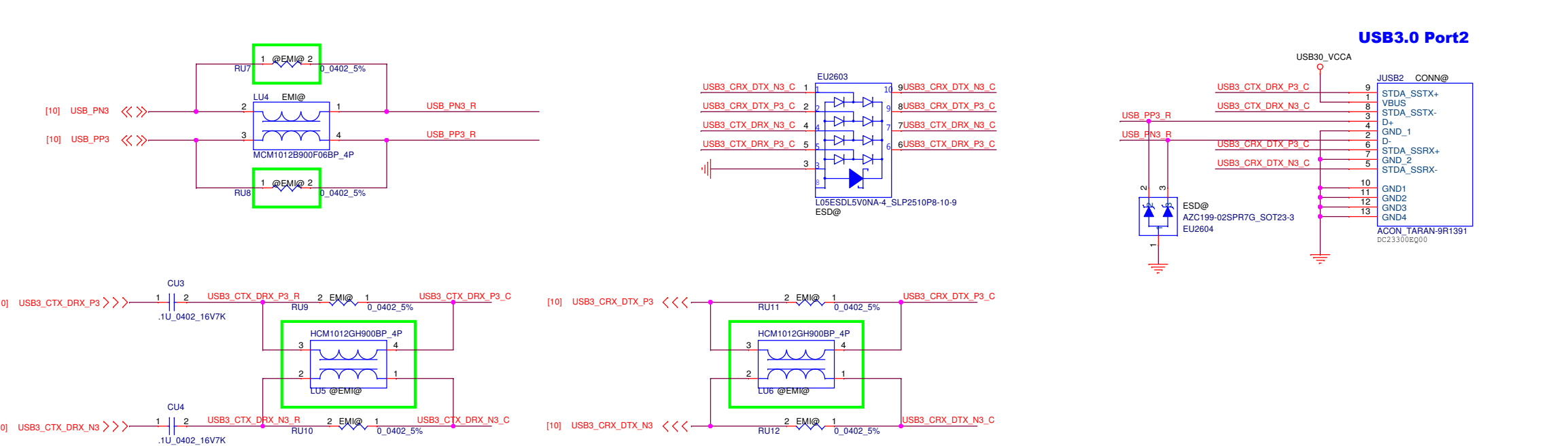
Layout Note: Close JUSB1



Layout Note: Close JUSB2

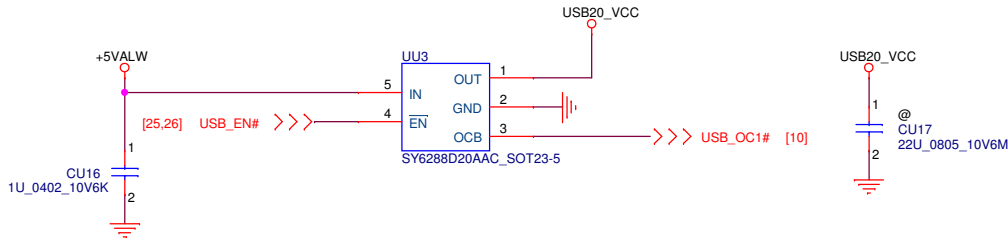


Main Func = USB3.0 Port2

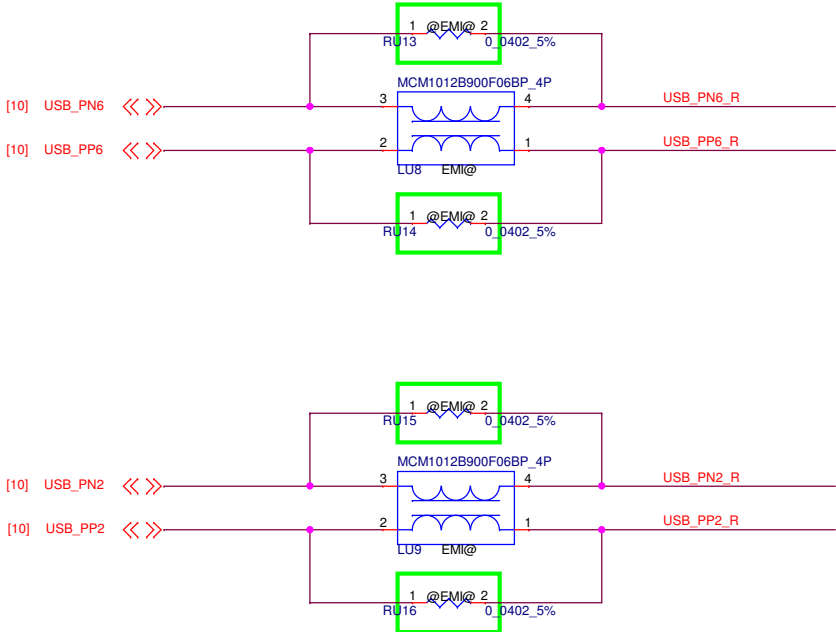


Main Func = USB2.0 + Card Reader on IO/B

SY6288D Support 2A

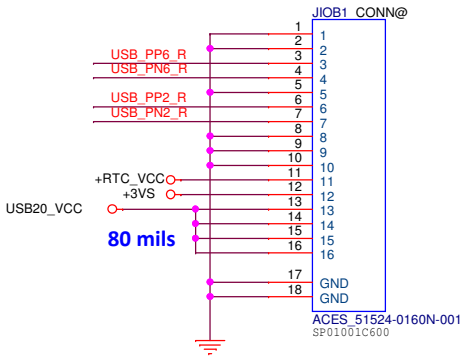


CardReader

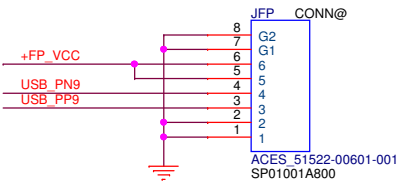
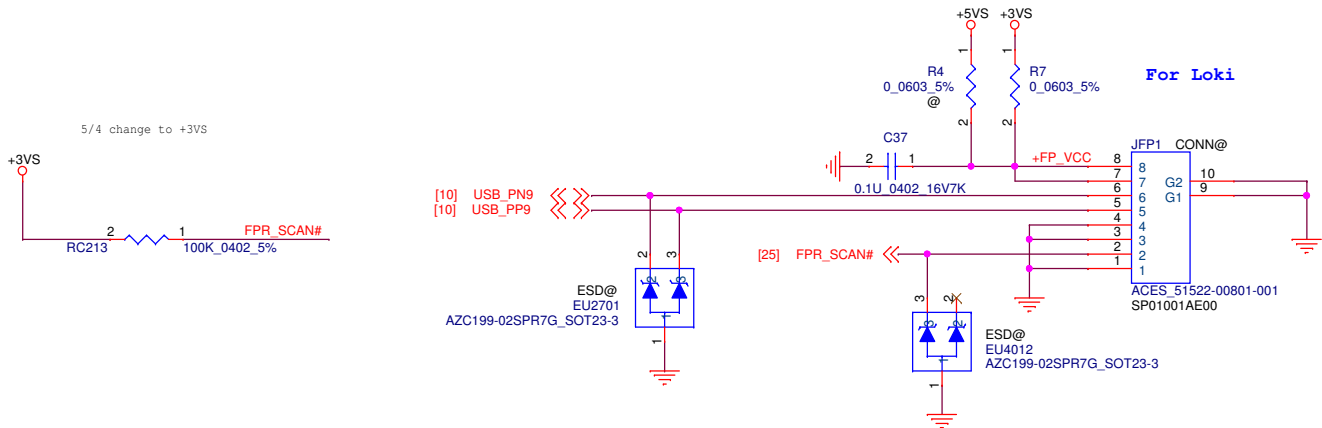


I/O Board Connector

CardReader



Main Func = Finger Printer

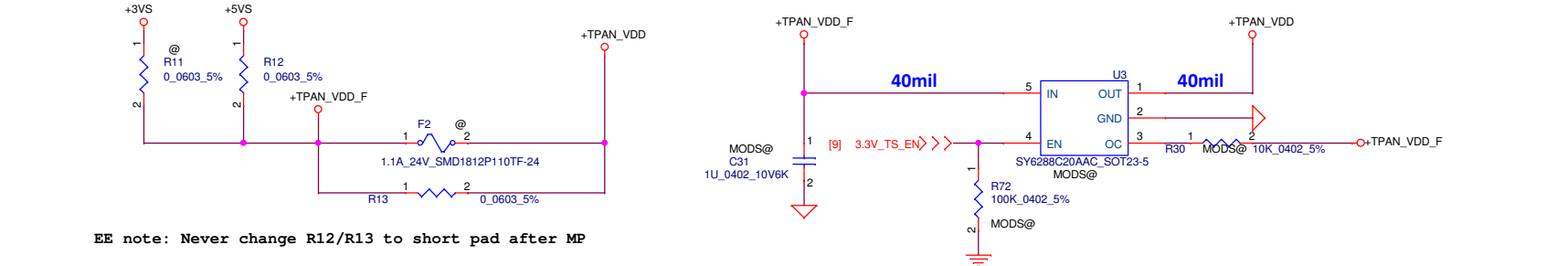
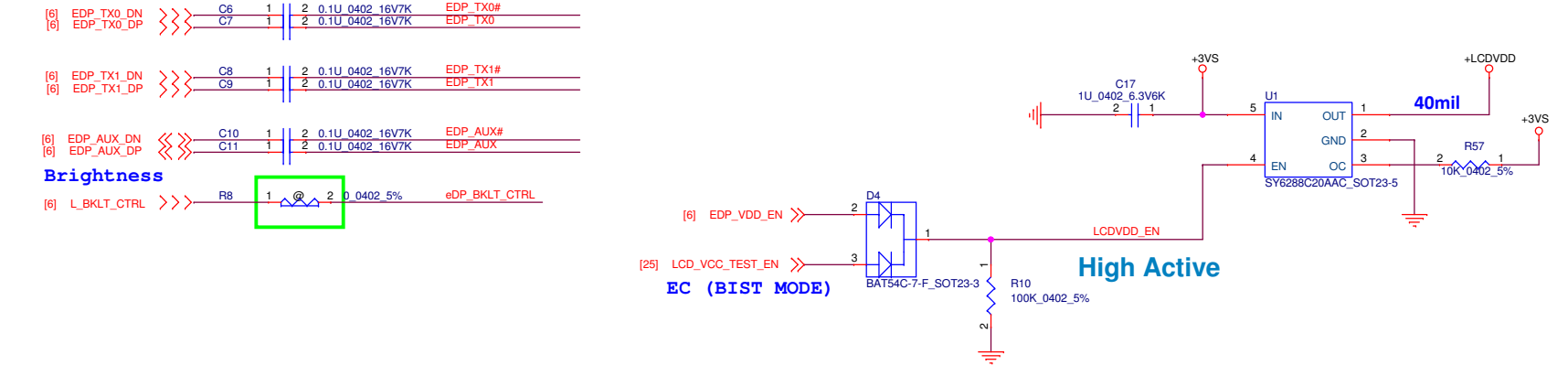
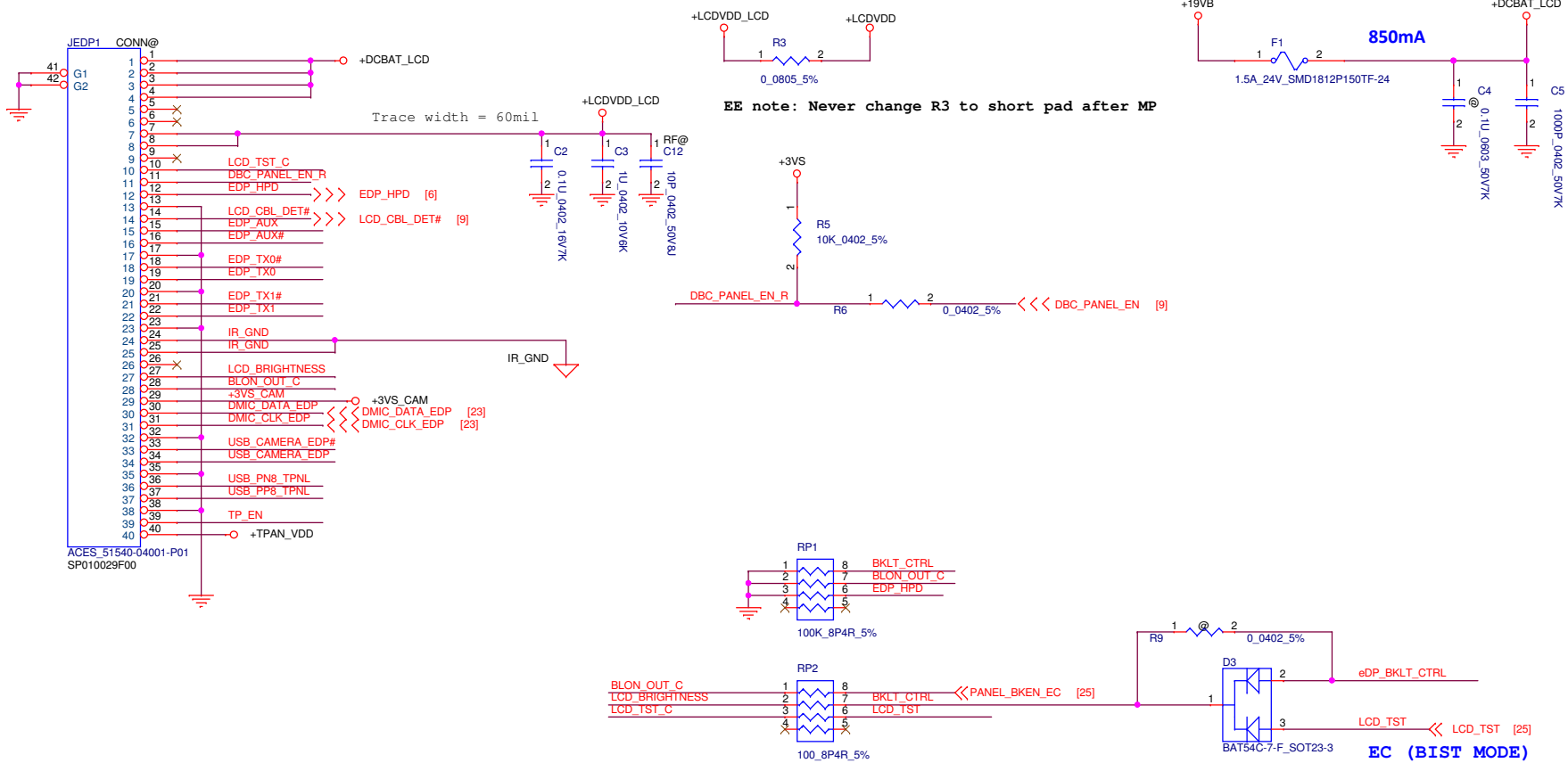


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				Size	Document Number	Rev
				C	LA-F114P	A00
				Date:	Wednesday, July 26, 2017	Sheet 27 of 54

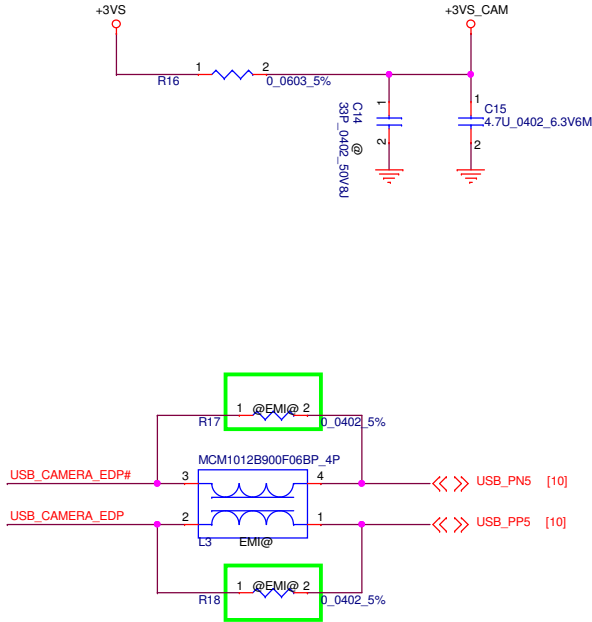
Main Func = LCD

INVERTER POWER

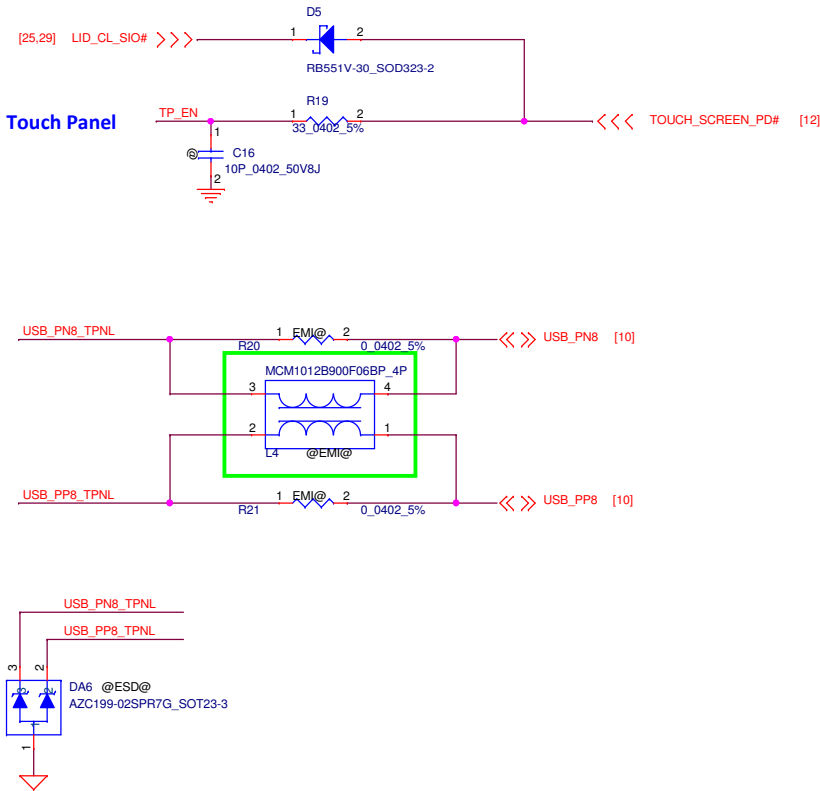
Main Func = CAM



EE note: Never change R16 to short pad after MP

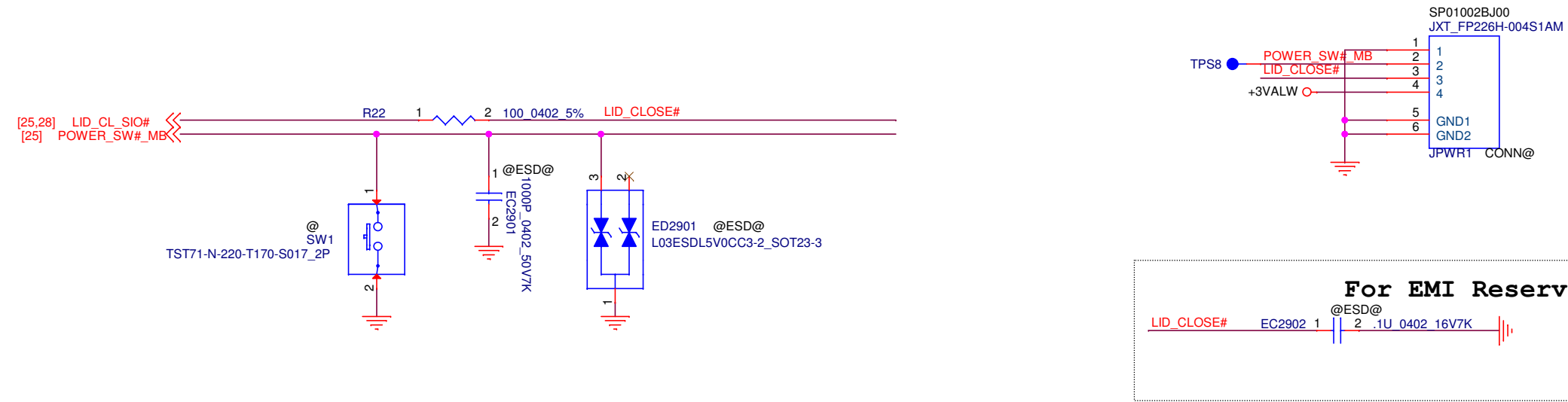


Main Func = TS



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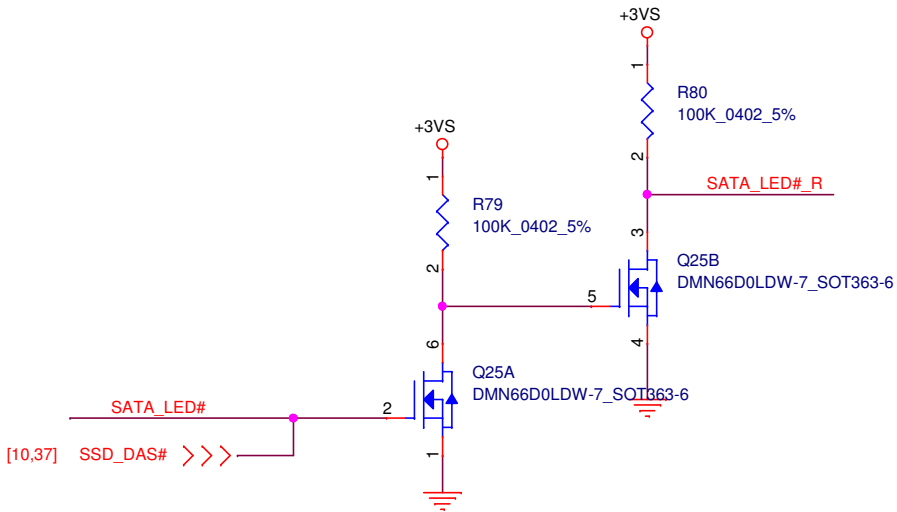
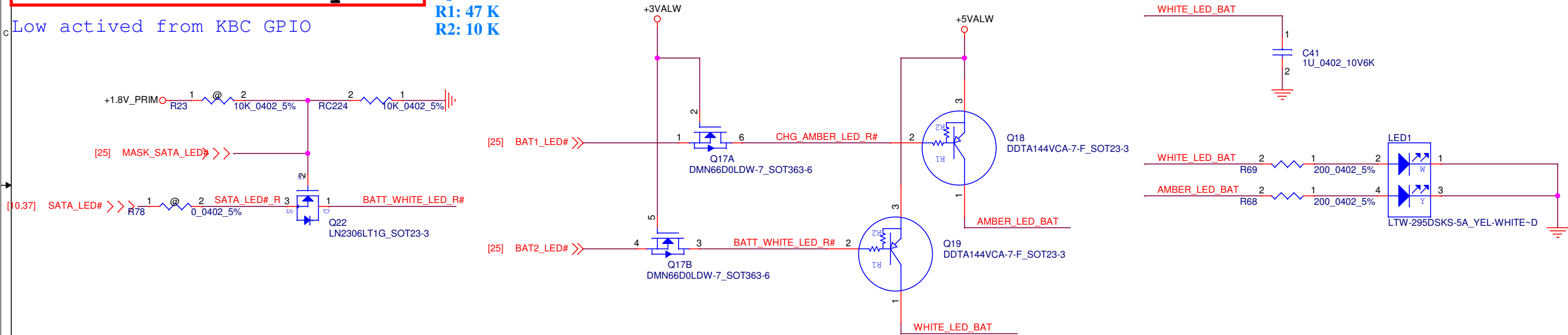
Main Func = Power BTN



Main Func = Battery LED

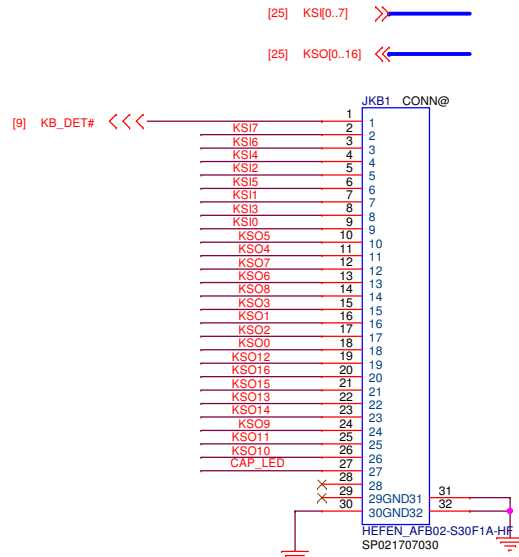
Low actived from KBC GPIO

BJT  
R1: 47 K  
R2: 10 K

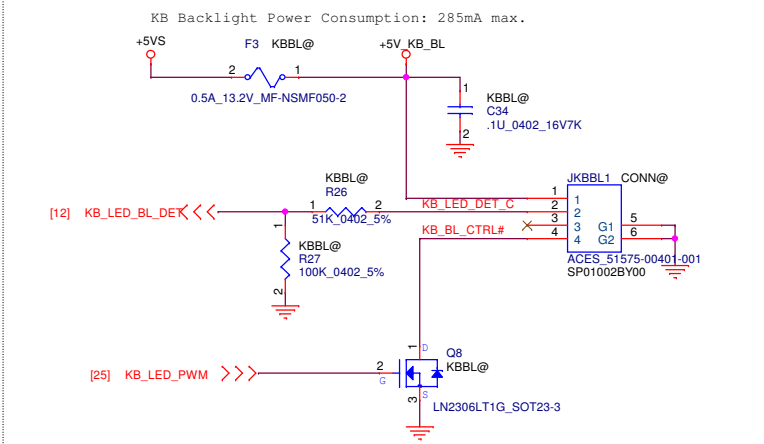


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Document Number				Rev	A00
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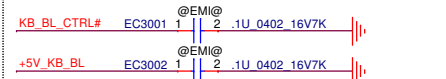
Main Func = KB



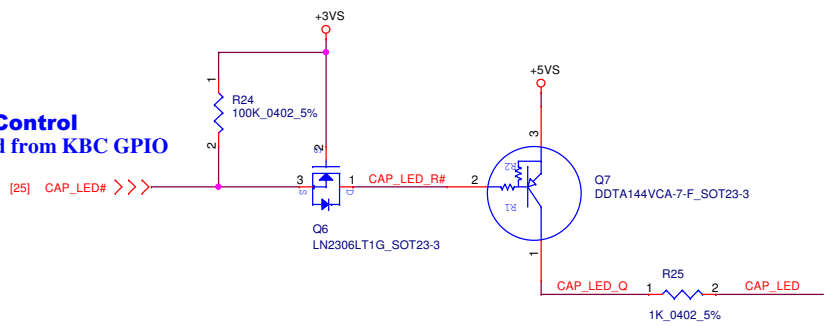
Keyboard Backlight (Reserved)



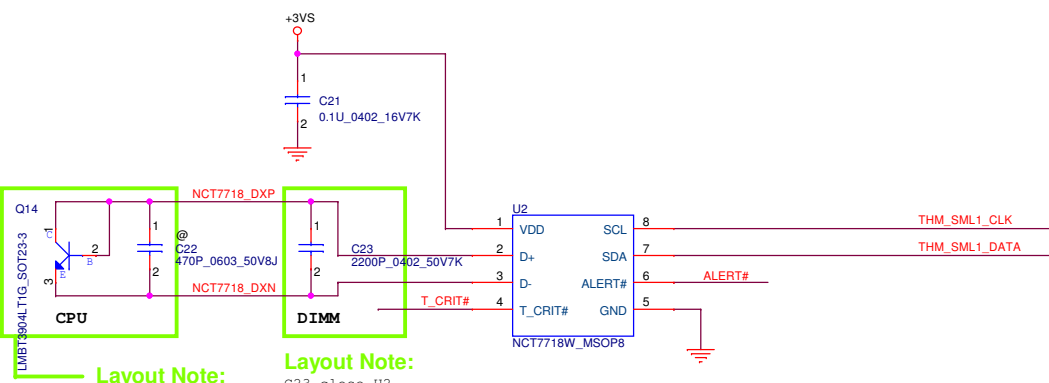
For EMI Reserved



CAP LED Control  
LOW acted from KBC GPIO



Main Func = Thermal

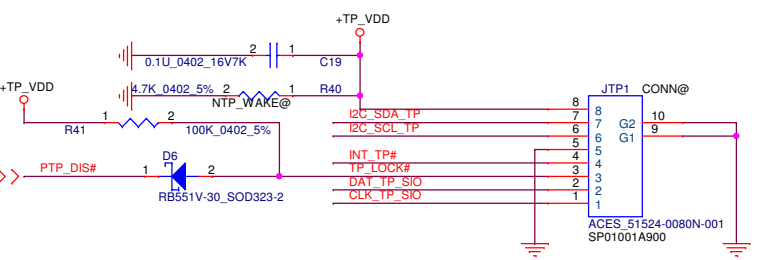
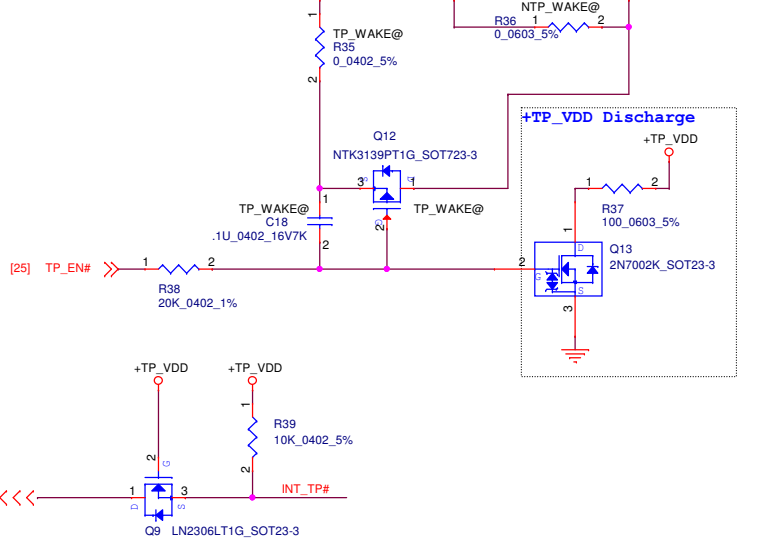
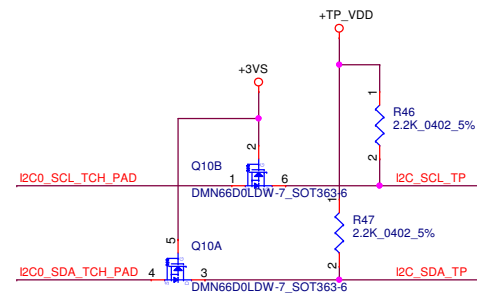
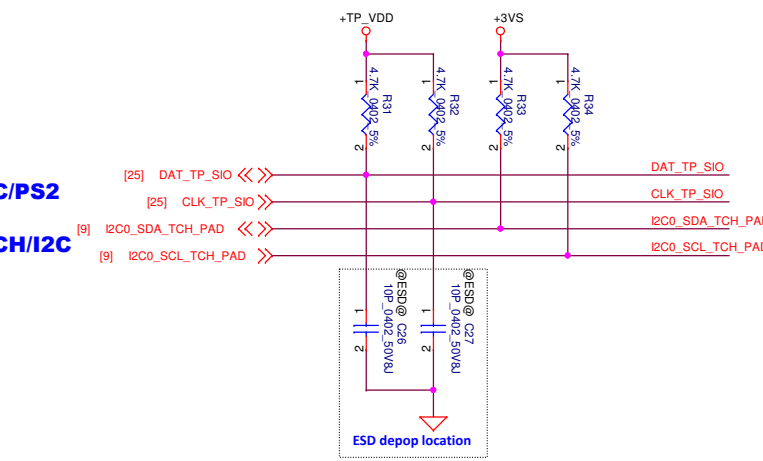


DXN and DXP routing width and spacing is 10 mil / 10 mil.

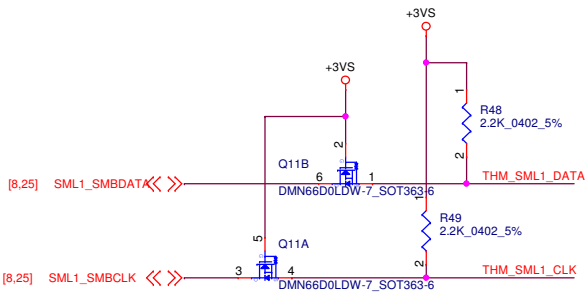
TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = TPAD

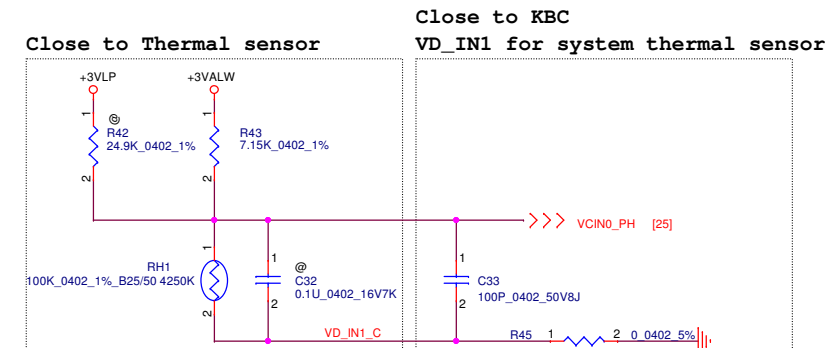
EC/PS2  
PCH/I2C



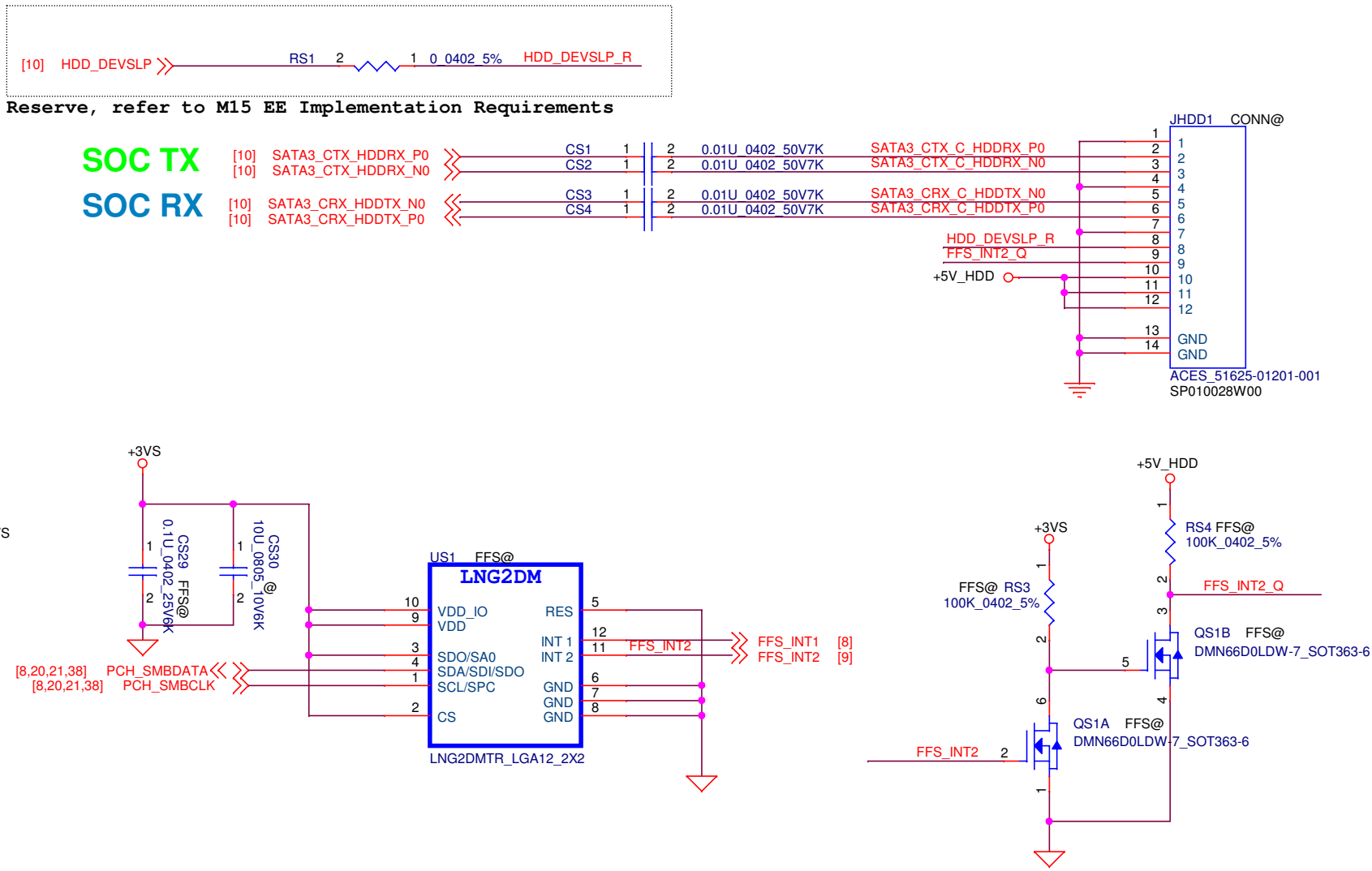
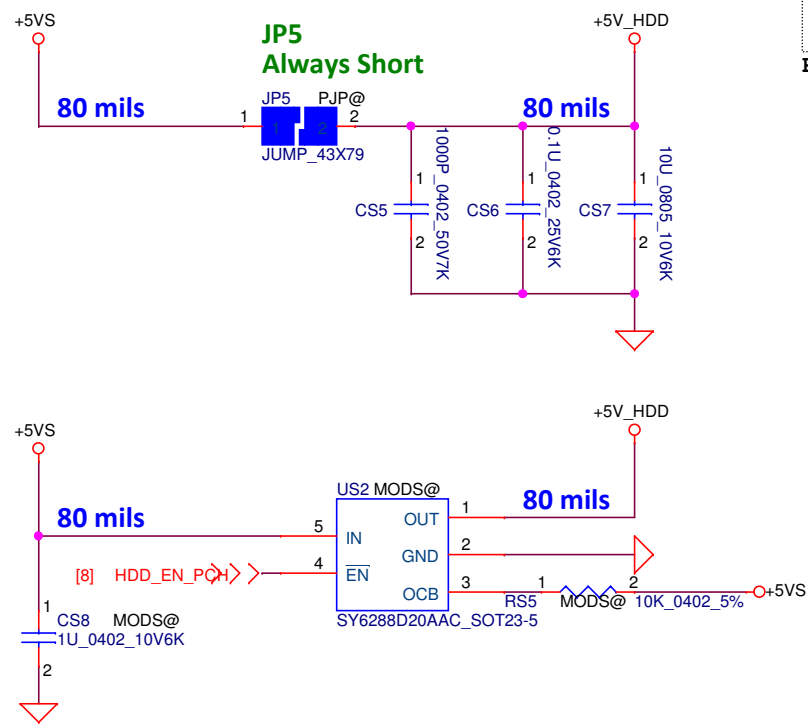
"FAN1\_TACH" PU 10k on EC side



Main Func = OTP

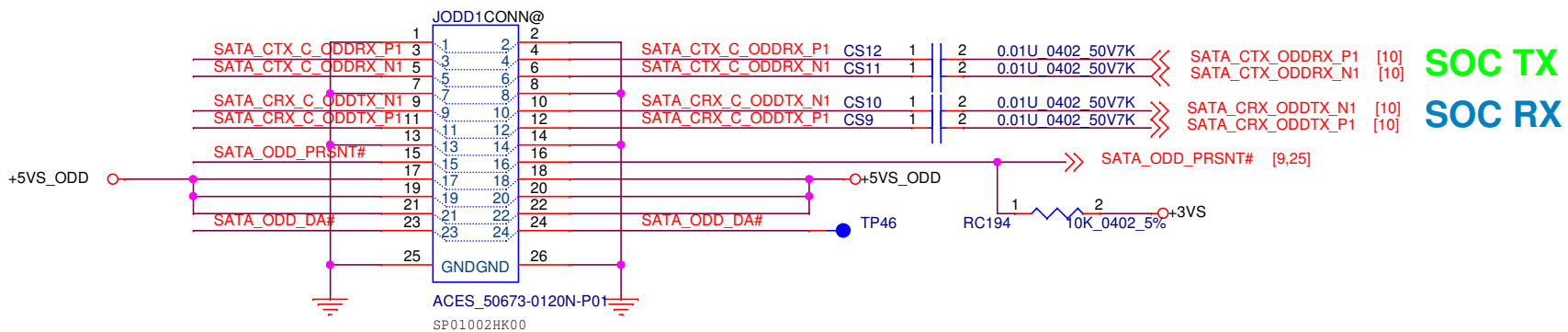
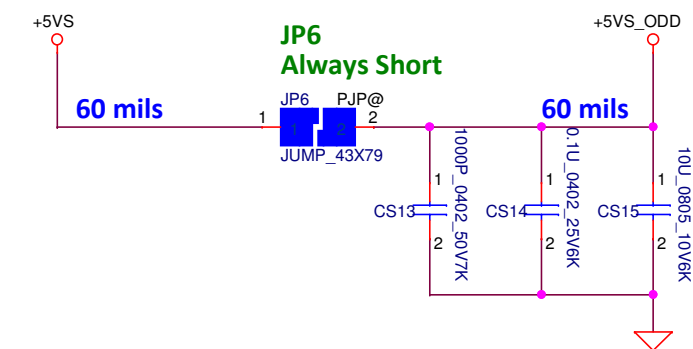


# Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

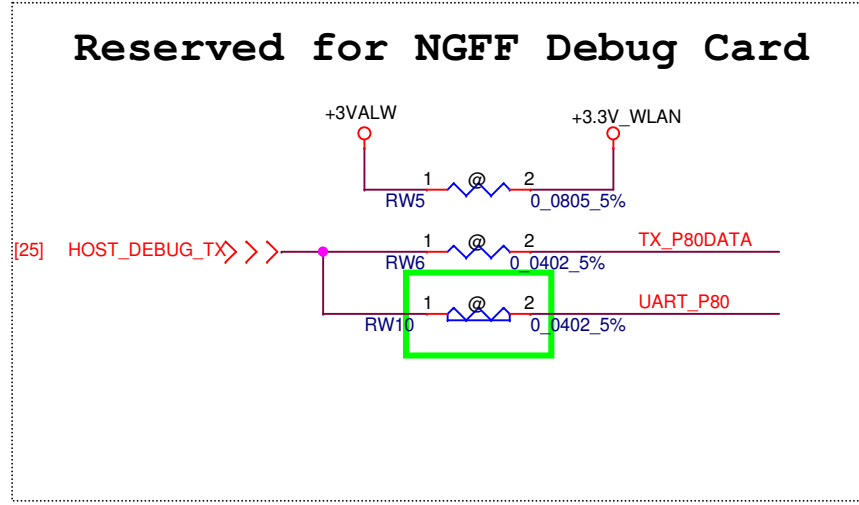
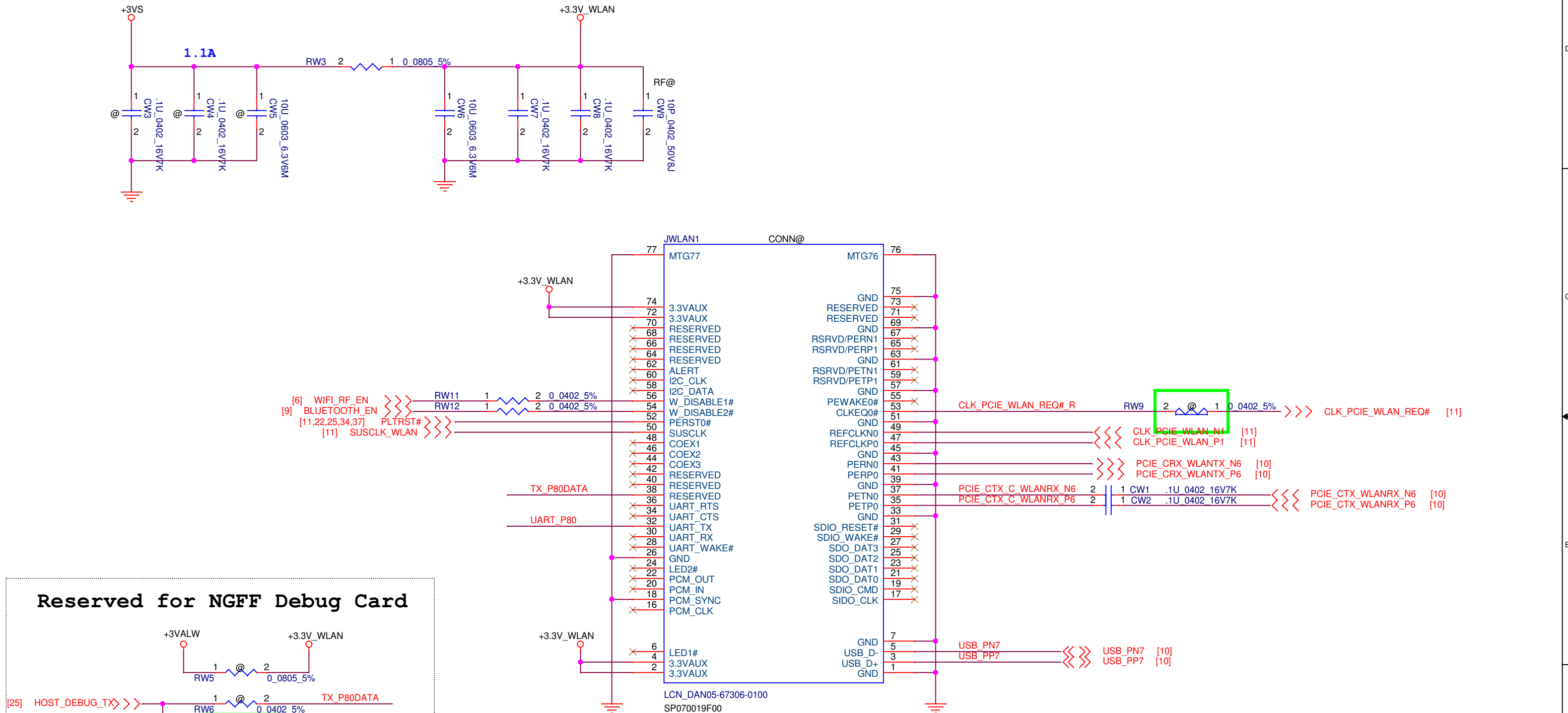
## Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSENT	P1	8
5V	P2	9
5V	P3	10 11
Attention	P4	12
GND	P5	
GND	P6	

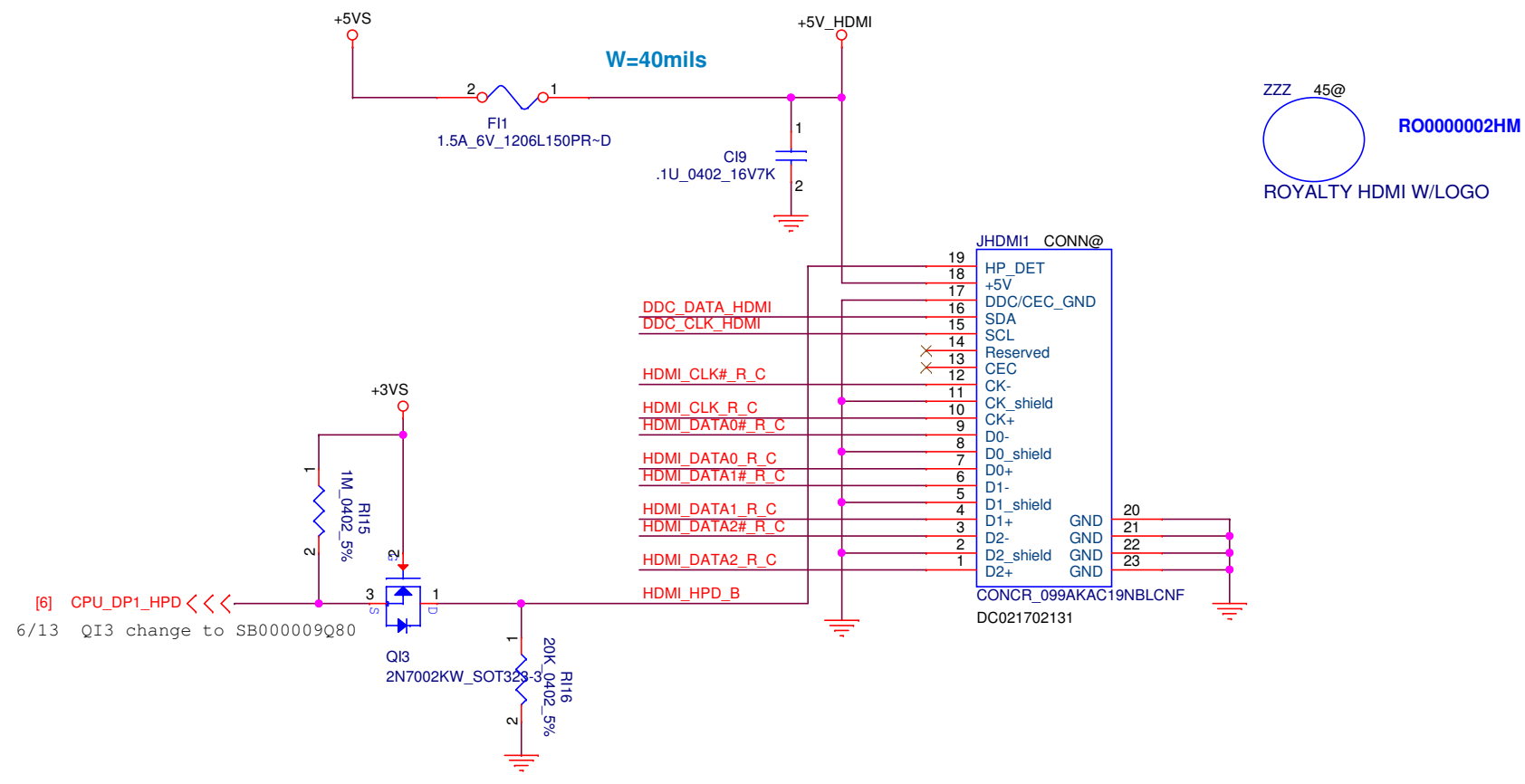
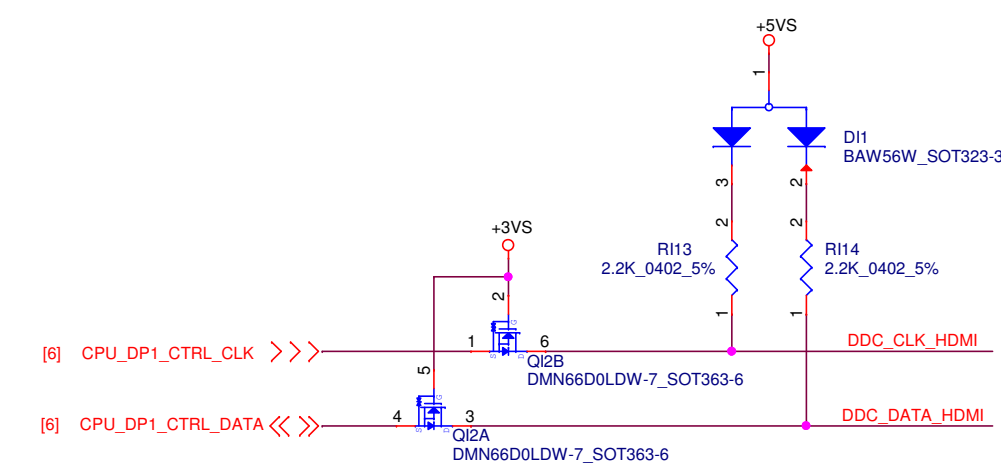
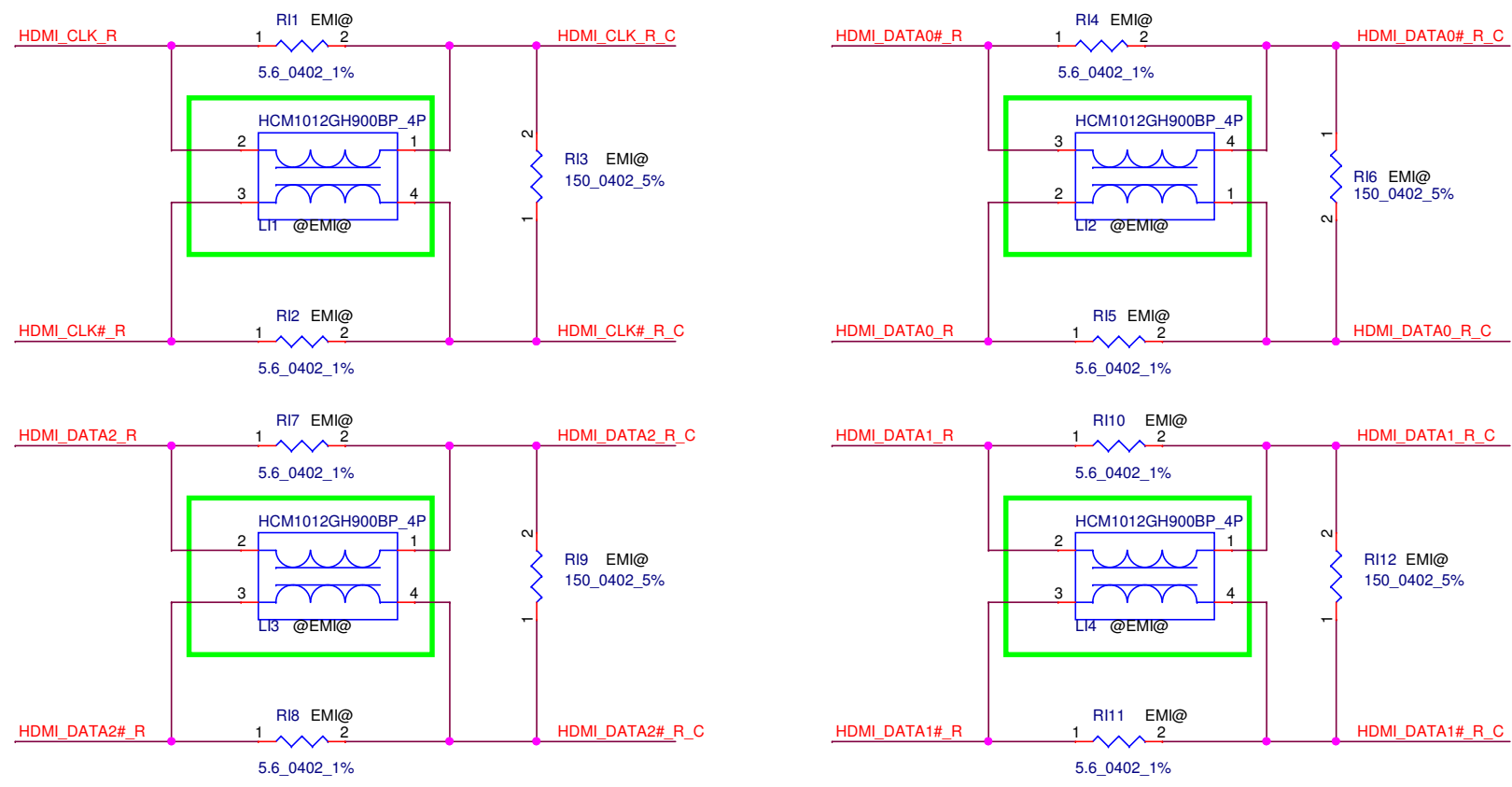
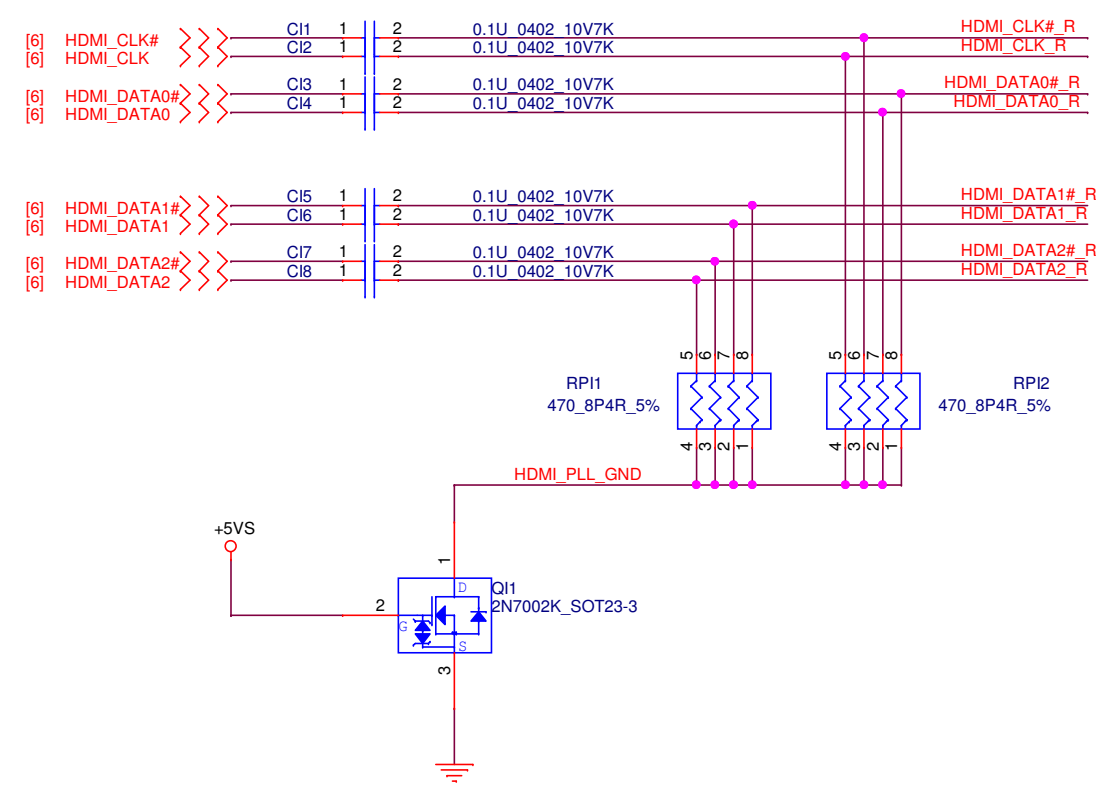
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					Final	Document Number		Rev	
					Size	Custom	<b>LA-F114P</b>		A00
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Main Func = WLAN A Key CONN



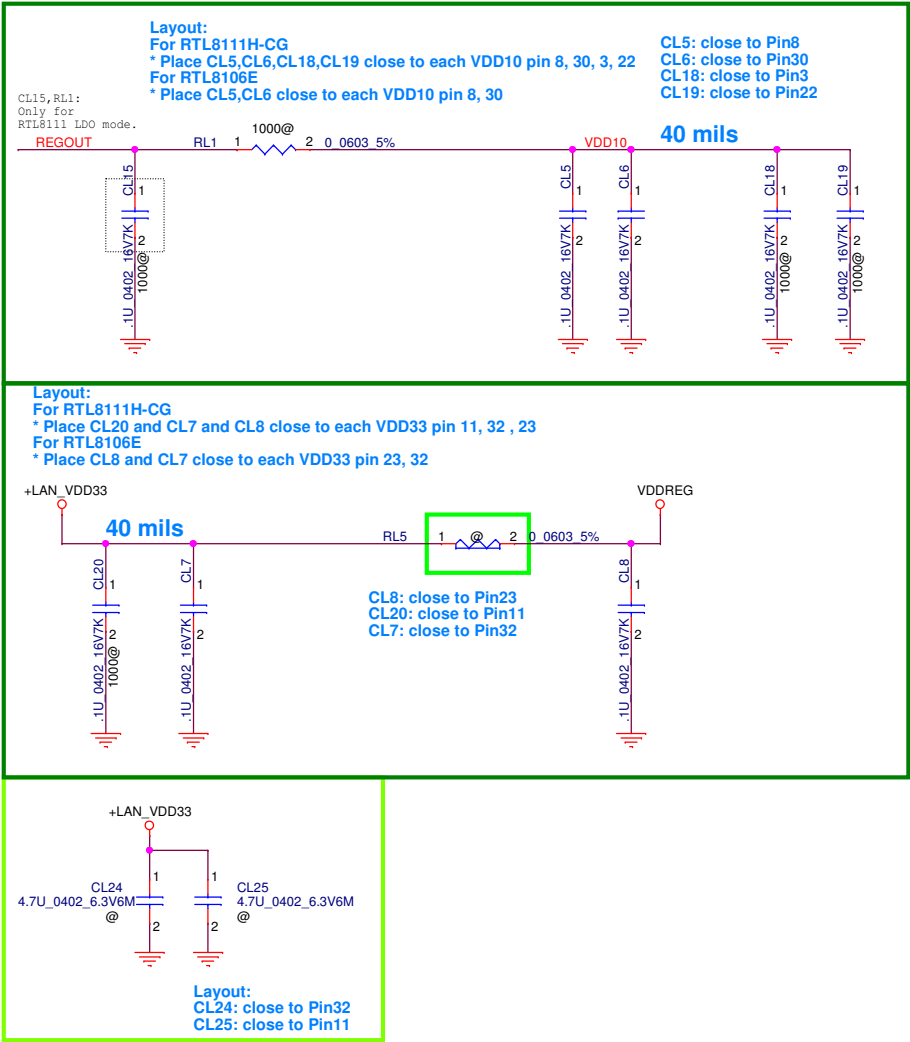
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				Rev	A00

Main Func = HDMI



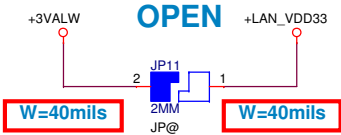
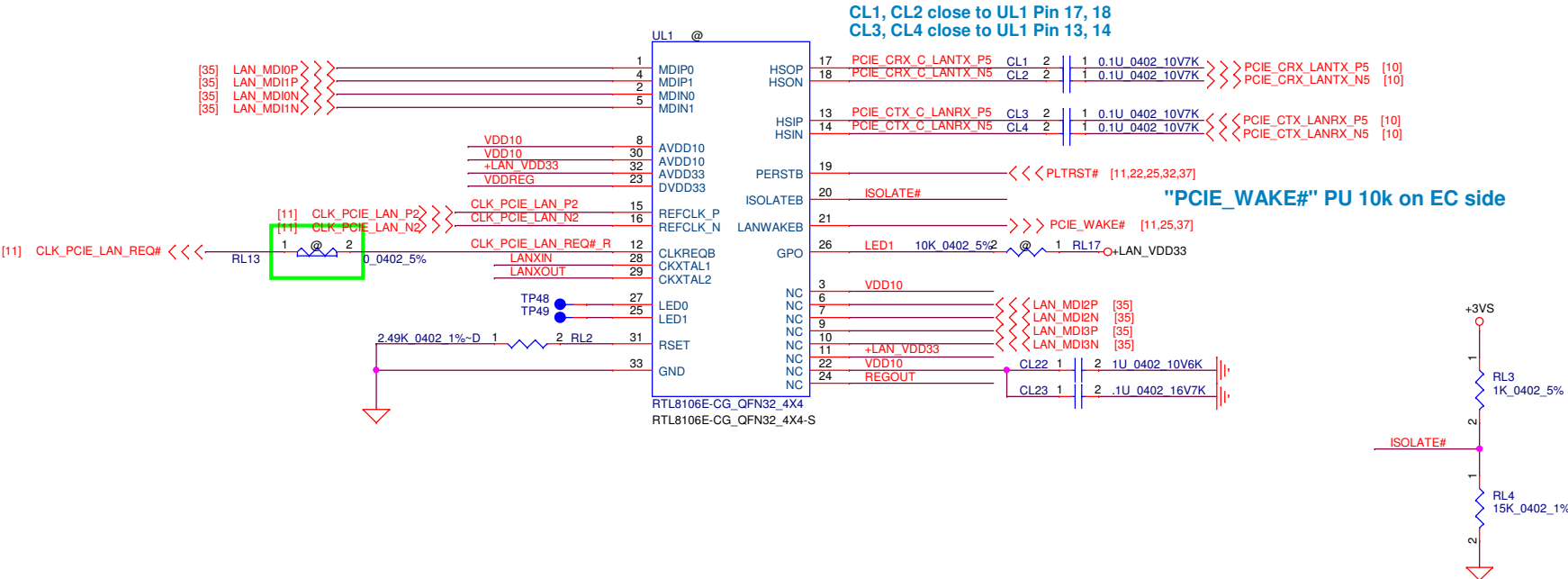
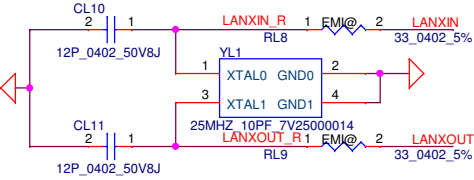
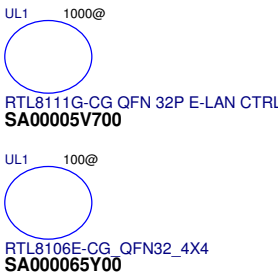
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Main Func = LAN

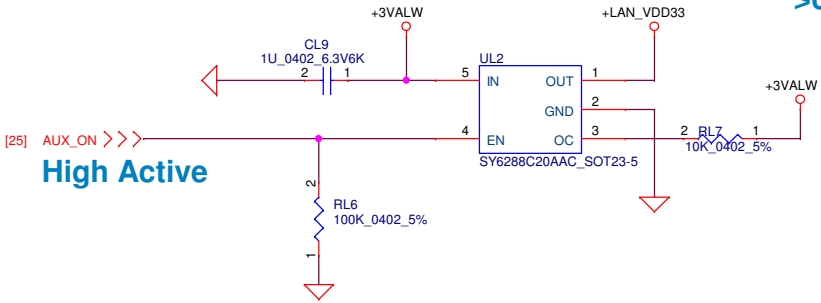


LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M



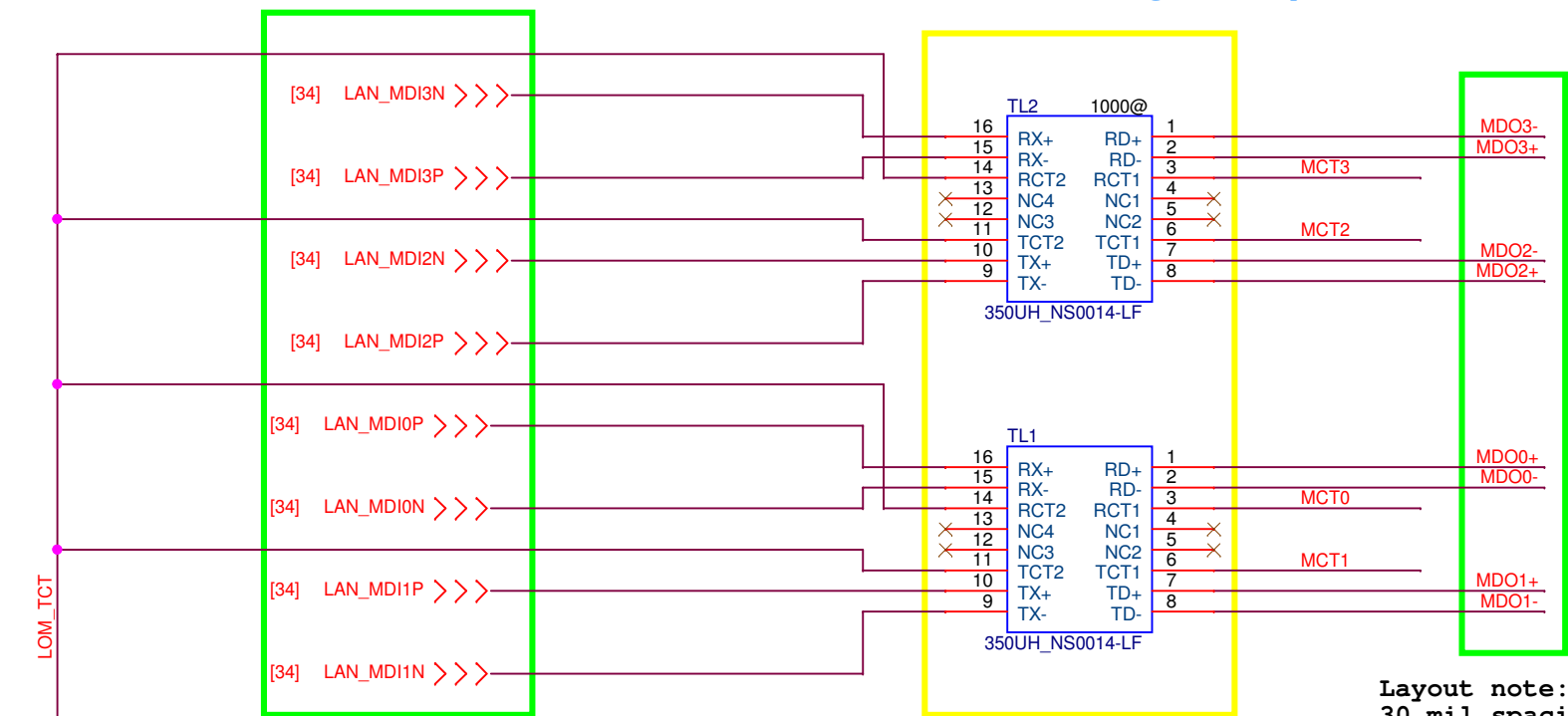
+LAN\_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Main Func = LAN LAN Transformer 10/100M x2

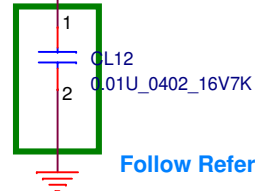
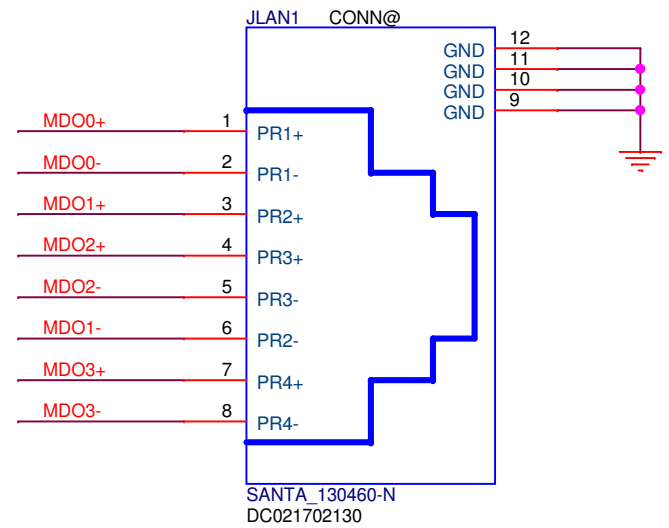
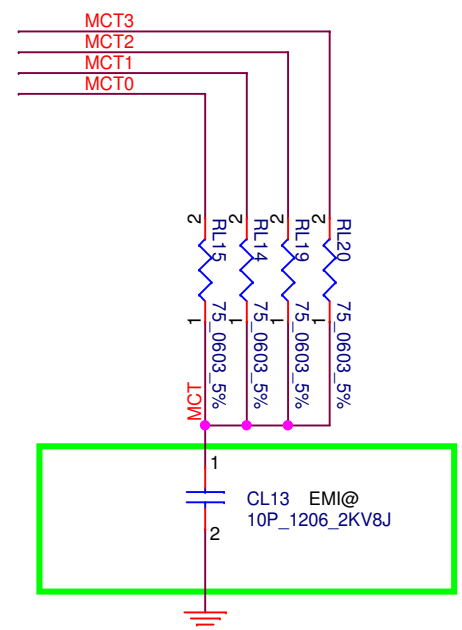
TL1 TOP, TL2 BOT  
2/24 change footprint



Layout note:  
30 mil spacing between MDI differential pairs.

Layout note:  
30 mil spacing between MDI differential pairs.

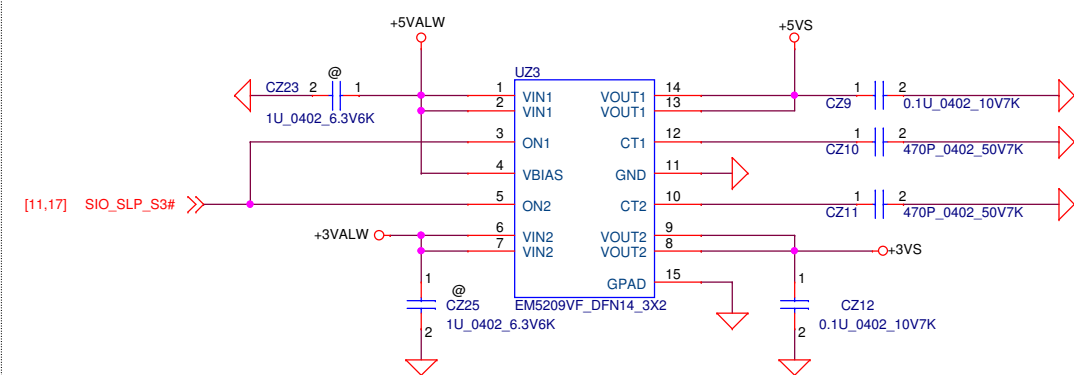
Main:  
SP050006H00, S X'FORM\_ NS0014 LF LAN  
2nd:  
SP050006W00, S X'FORM\_ HD-245 10/100 PC CARD LAN



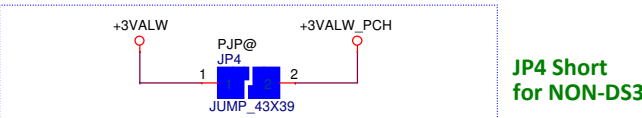
Follow Reference Schematic 0.01uF~0.4uF

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+5VS/+3VS for System

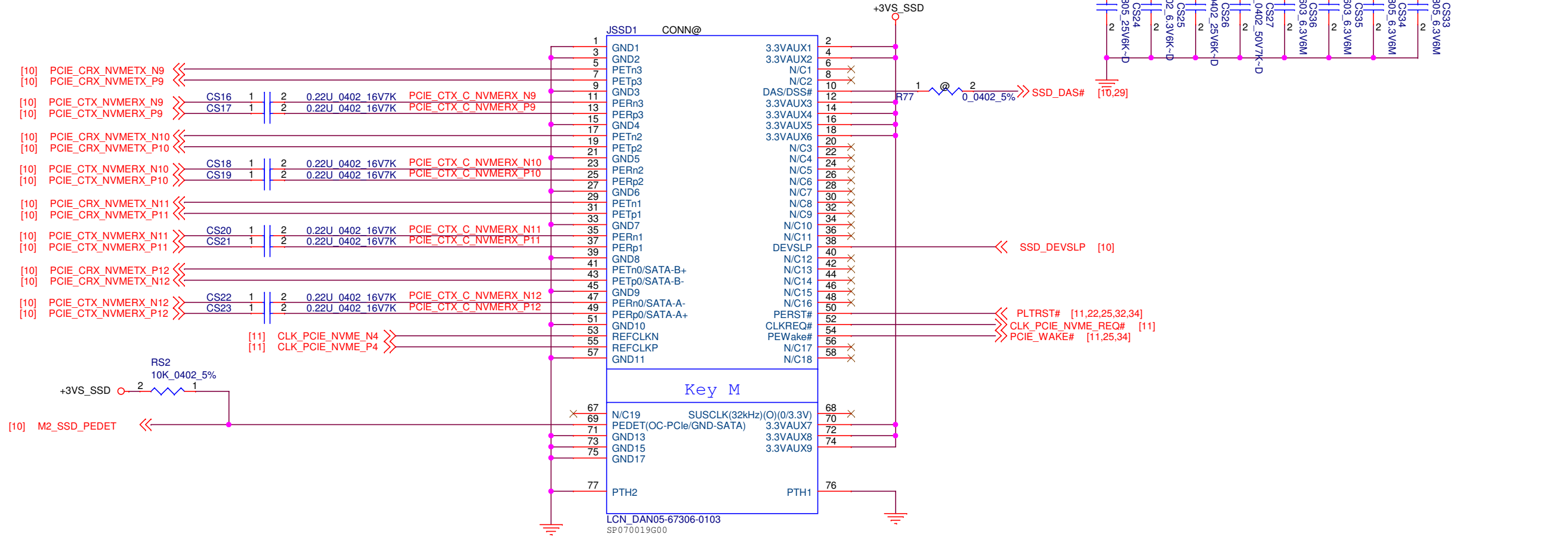


+3VALW\_PCH for System



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NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Main Func = VGA/B

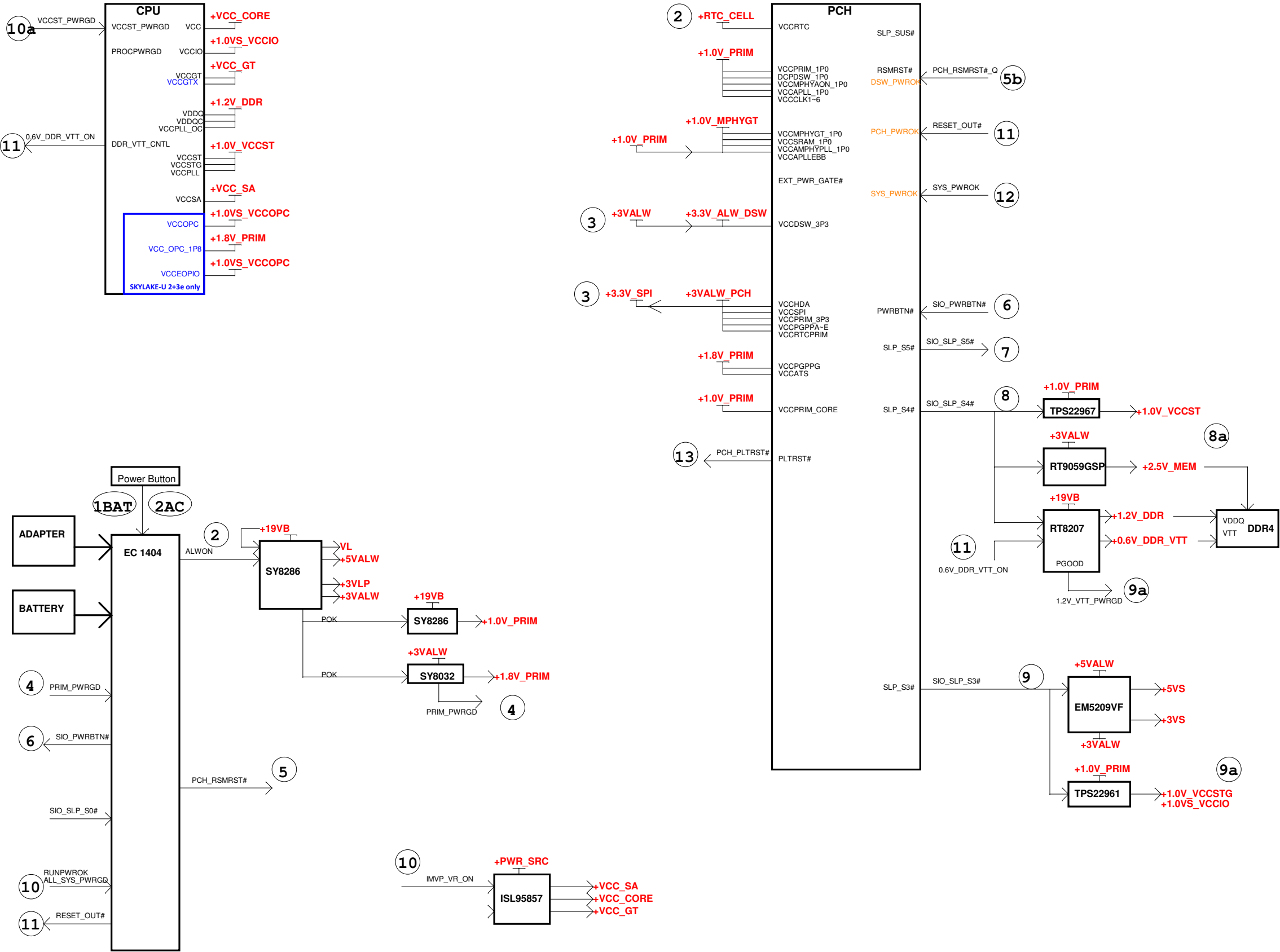


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				Size B	Rev A00
Date: Wednesday, July 26, 2017		Sheet 38 of 54		Document Number LA-F114P	

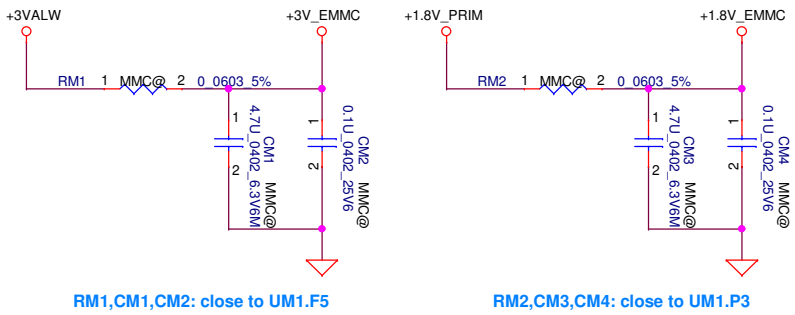
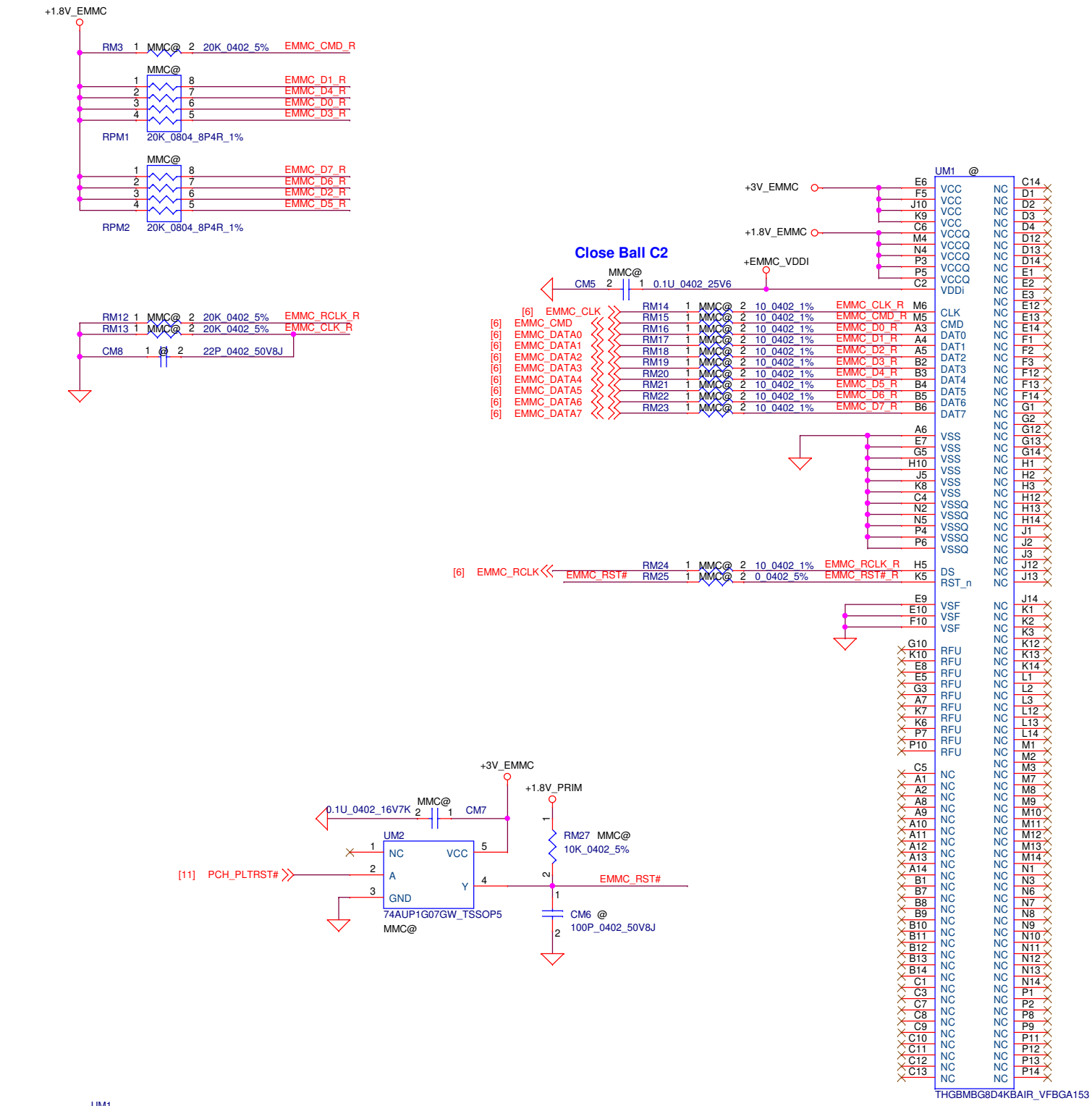
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				Size B	Document Number <b>LA-F114P</b>	Rev A00
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Timing Diagram for S5 to S0 mode



Main Func = eMMC



UM1  
HYNIX  
SA00009N50L  
HYNIX\_128G@  
S IC FL 128G H26M88002AMR FBGA 153P

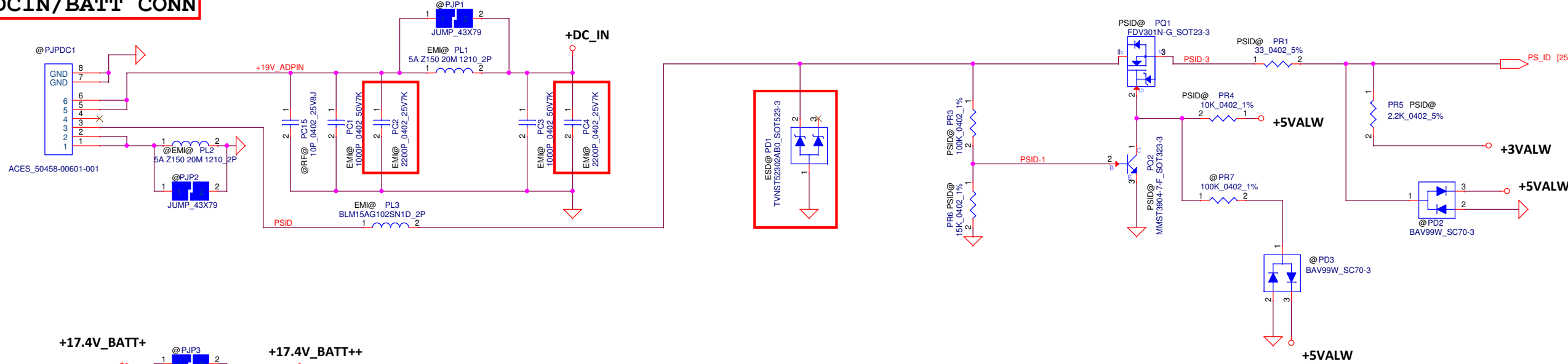
UM1  
SANDISK  
SA00009ML0L  
SANDISK\_128G@  
S IC FL 128G SDINADF4-128G-859 TFBGA

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				Size Custom
				Document Number LA-F114P
				Rev A00
				Date: Wednesday, July 26, 2017
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				Custom	A00
Date: Wednesday, July 26, 2017				Sheet	43 of 53

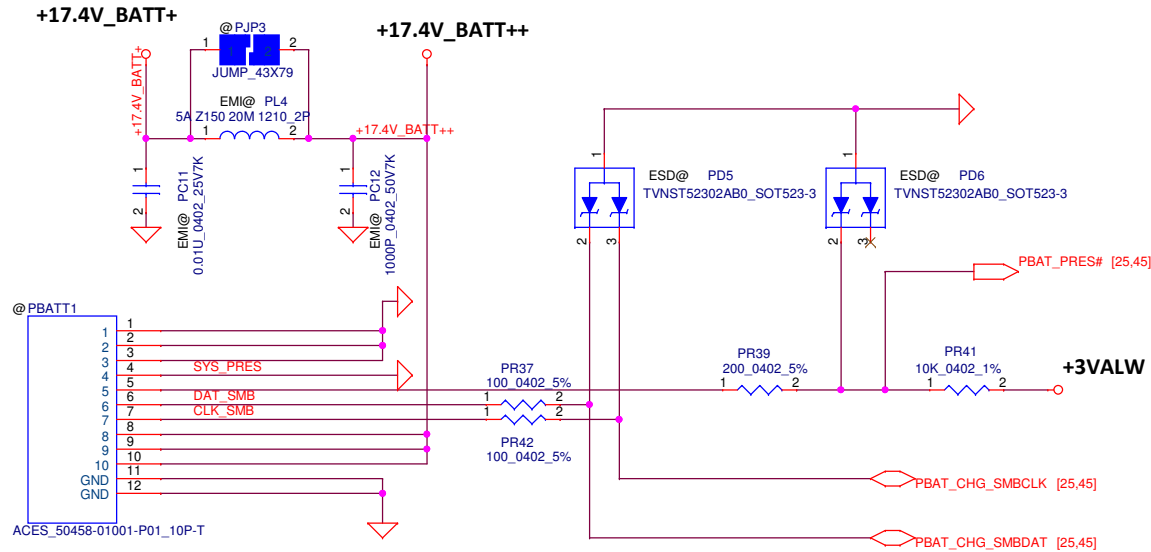
Main Func = DCIN/BATT CONN



Battery Bot Side

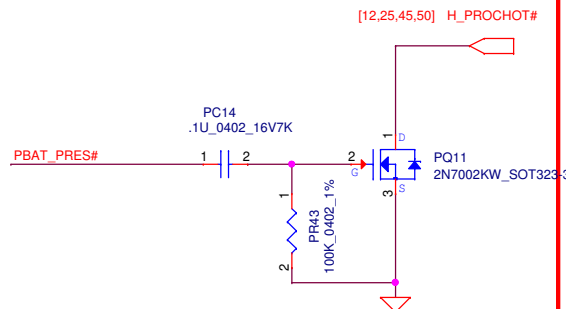
PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Batt+  
PIN9 Batt+  
PIN10 Batt+  
SP021412220

ACES\_50458-01001-P01\_10P-T



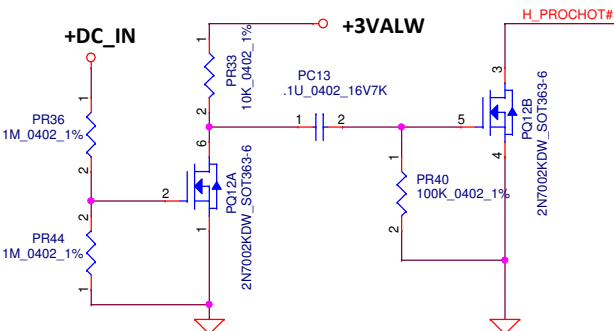
Adapter protection:

if battery removed, adaptor only,  
then trigger the H\_PROCHOT#,  
keep @ in BOM since battery can not  
be removed by end user

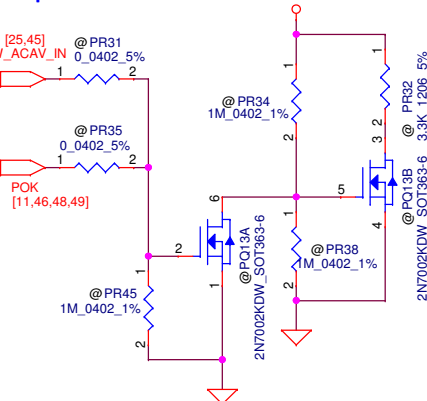


Battery protection:

asserts H\_PROCHOT# when adaptor is  
unplugged, keep low for 10ms  
till SW PROCHOT# is issued by EC



Erp lot6 Circuit

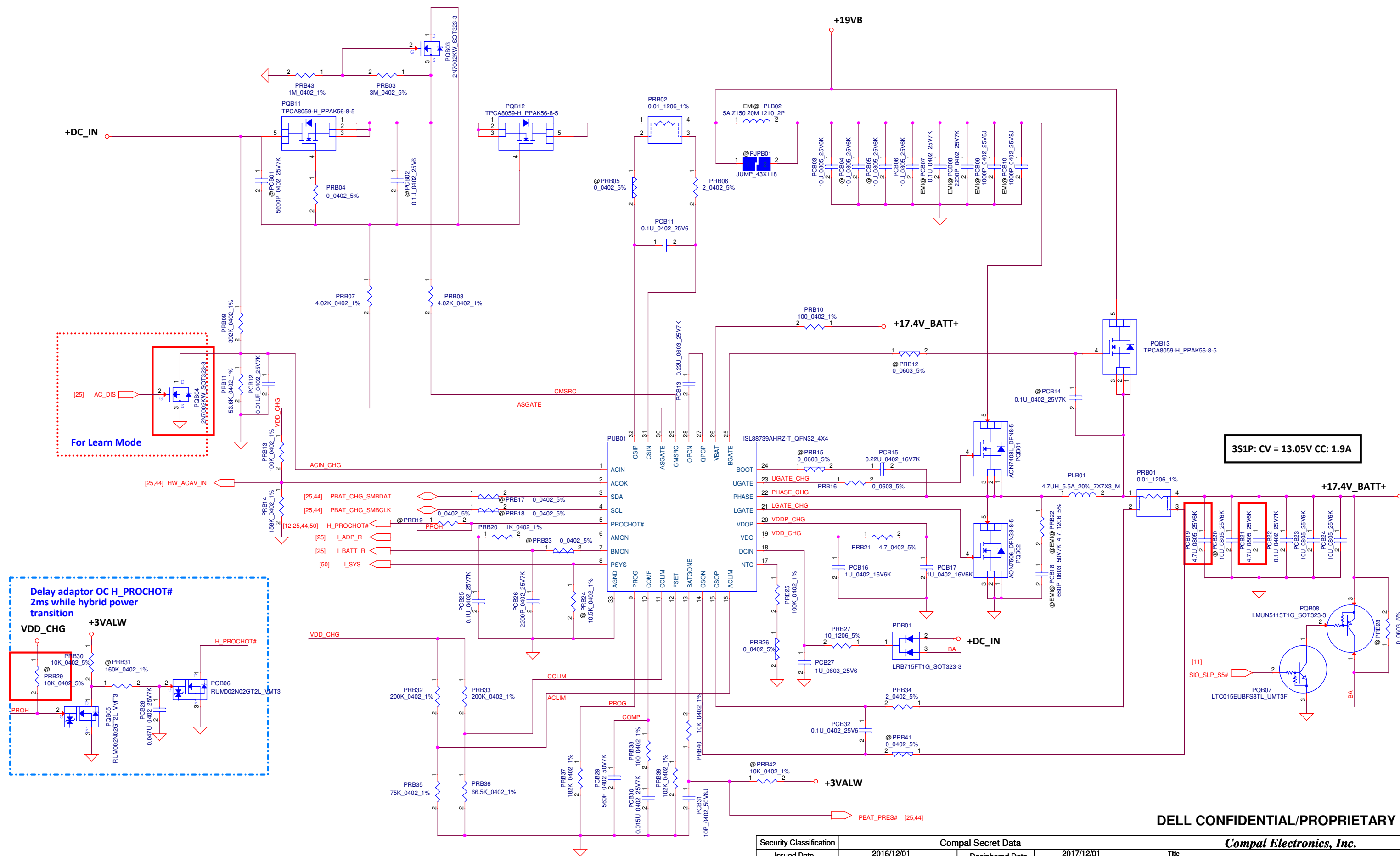


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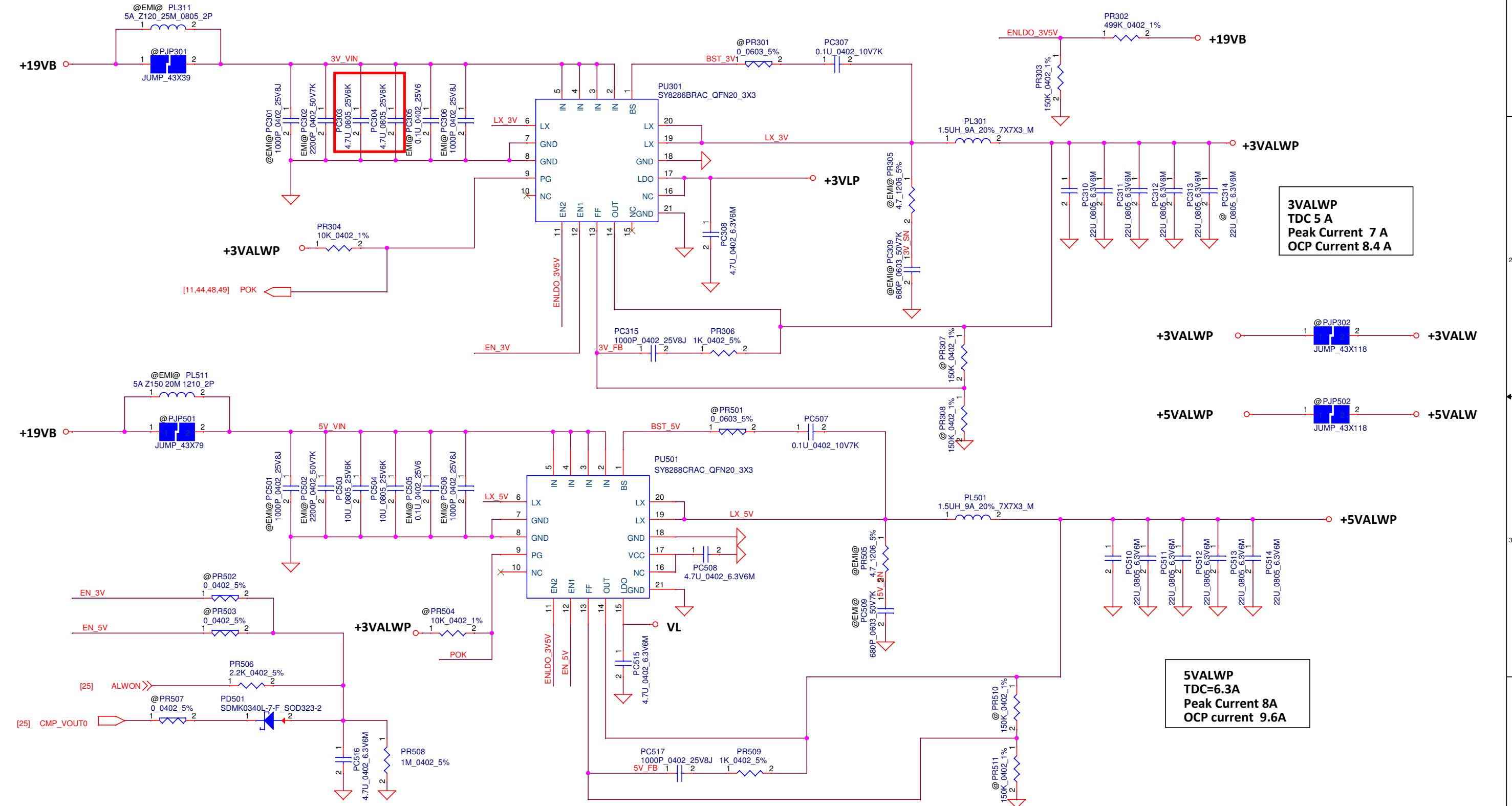
Main Func = CHARGER



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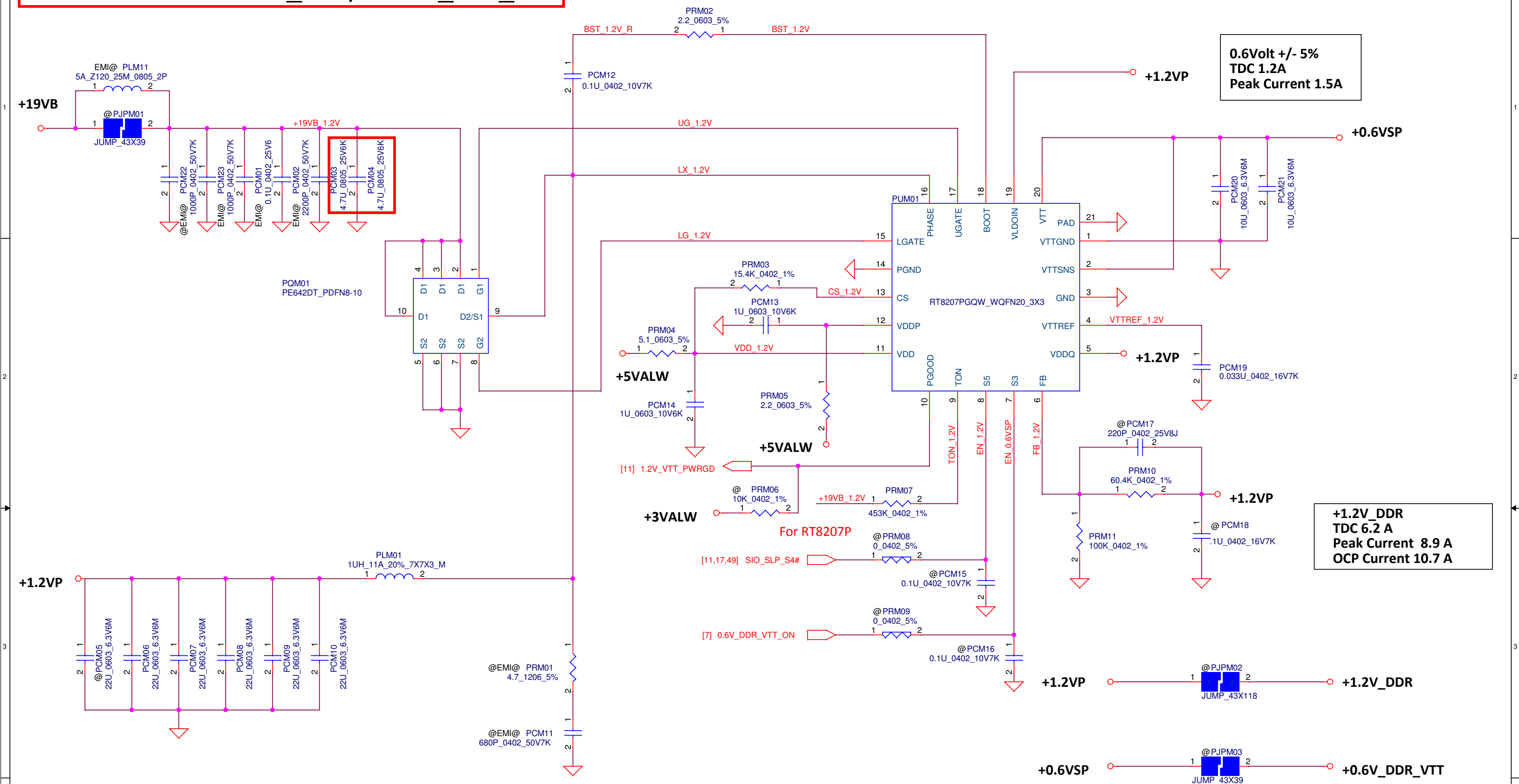
Security Classification		Compal Secret Data		Title	
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Main Func = 3.3VALWP/5VALWP



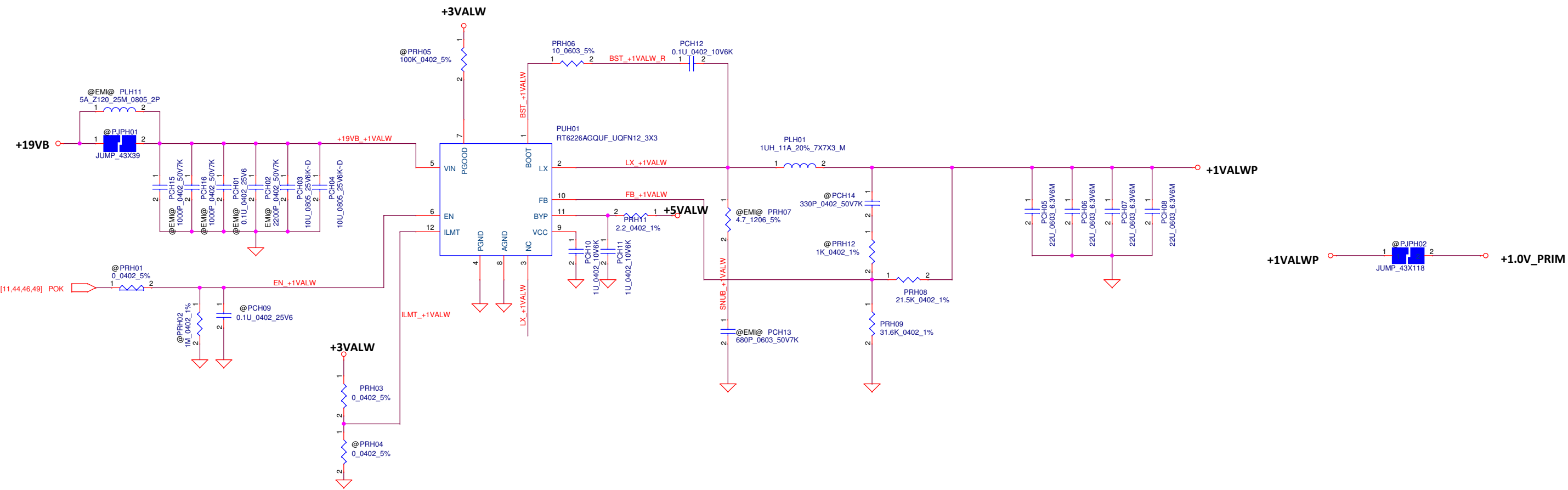
Security Classification		Compal Secret Data		Title	
Issued Date	2016/12/01	Deciphered Date	2017/12/01	Compal Electronics, Inc.	
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**Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT**



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						Size		Document Number		Rev	
						Custom				X00	
						Date:		Wednesday, July 26, 2017		Sheet 47 of 53	

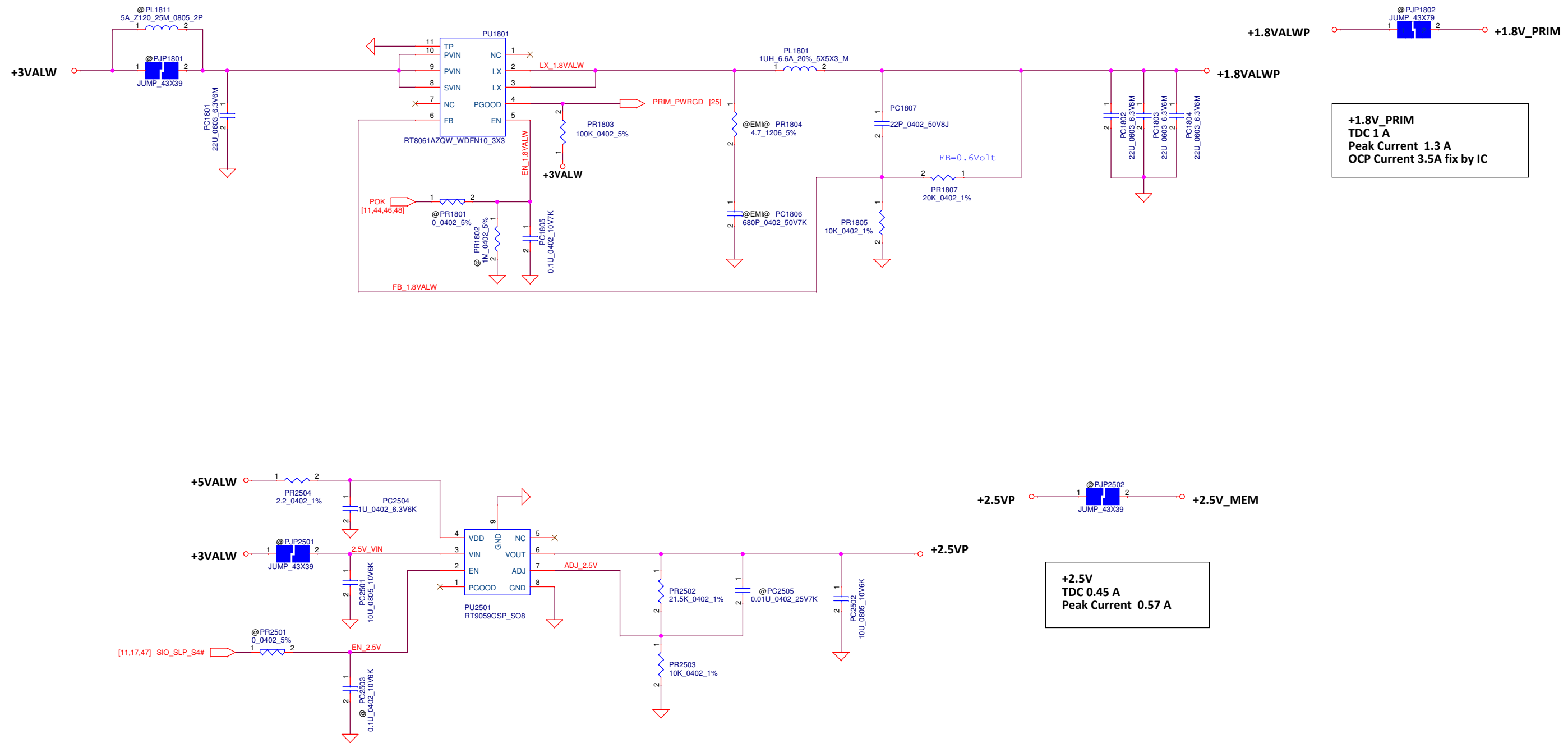
Main Func = +1VALWP



+1.0V\_PRIM  
TDC 5.2 A  
Peak Current 6.5 A  
OCP Current 9 A Fix by IC

Security Classification		Compal Secret Data		Title	
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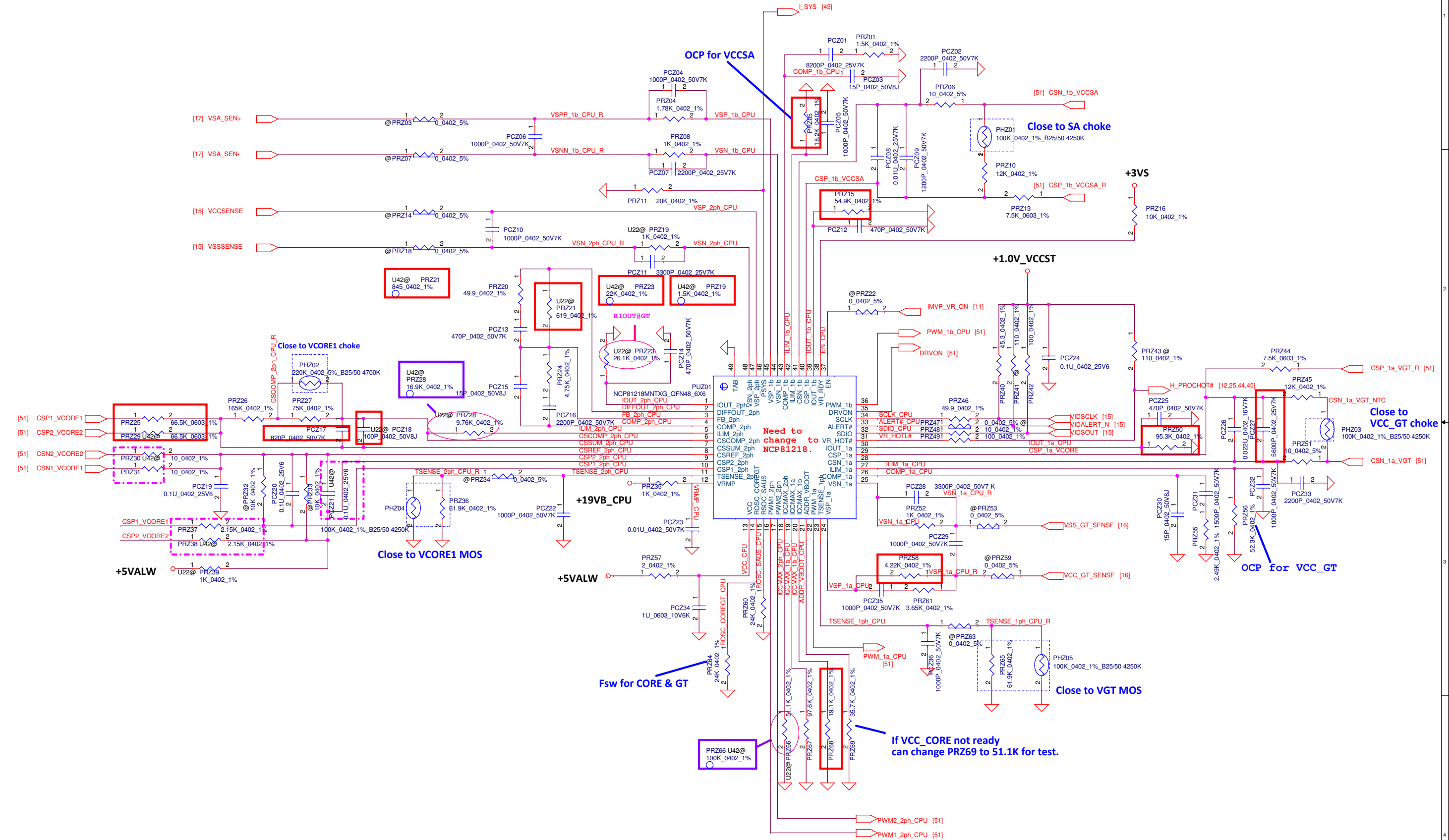
Main Func = +1.8VALWP / +2.5VP



+1.8V\_PRIM  
TDC 1 A  
Peak Current 1.3 A  
OCP Current 3.5A fix by IC

+2.5V  
TDC 0.45 A  
Peak Current 0.57 A

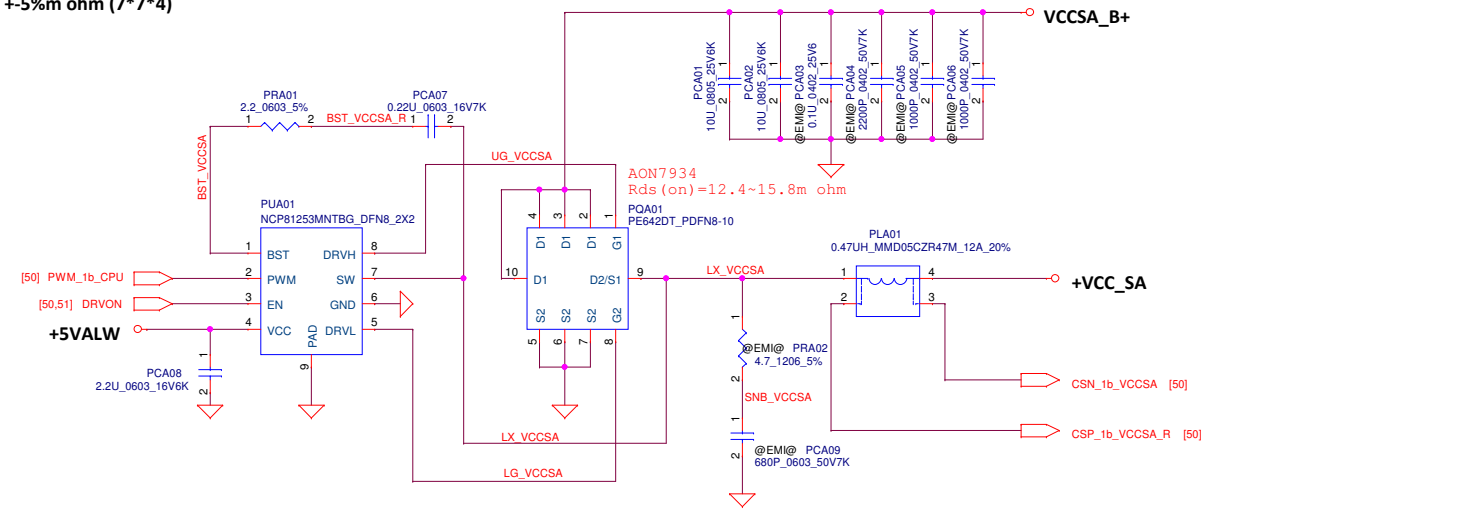
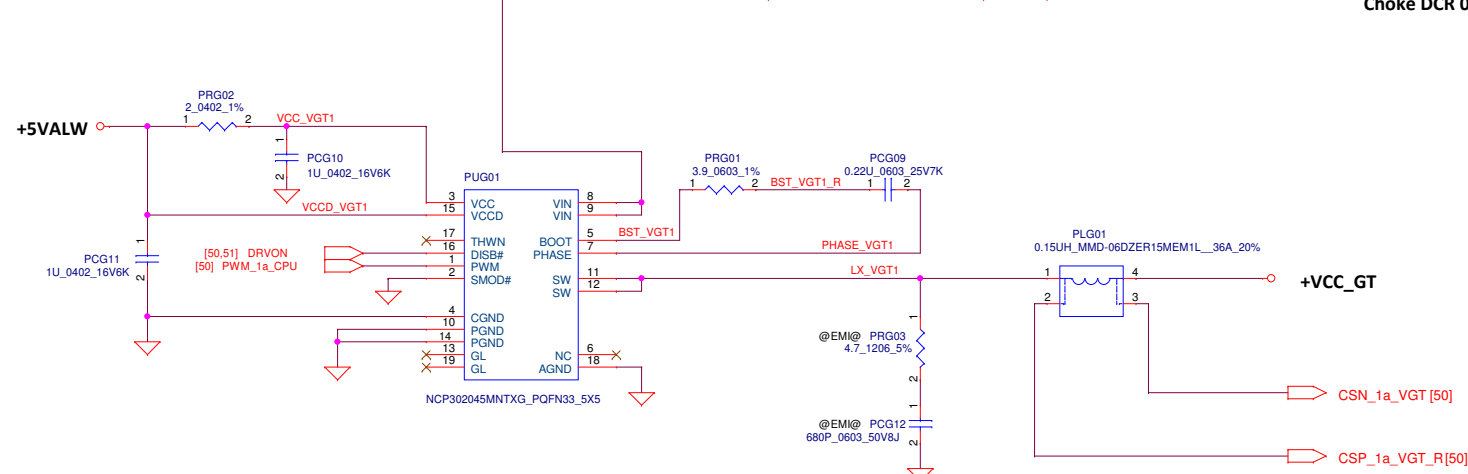
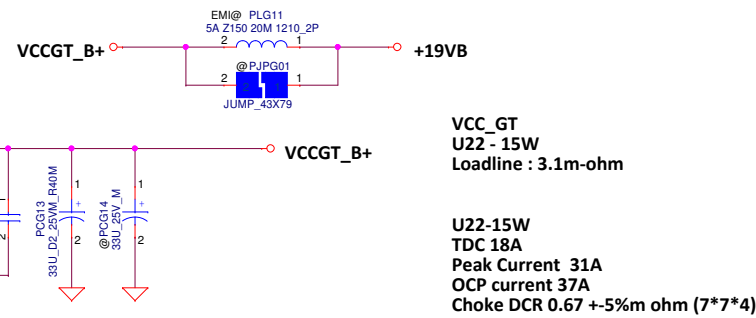
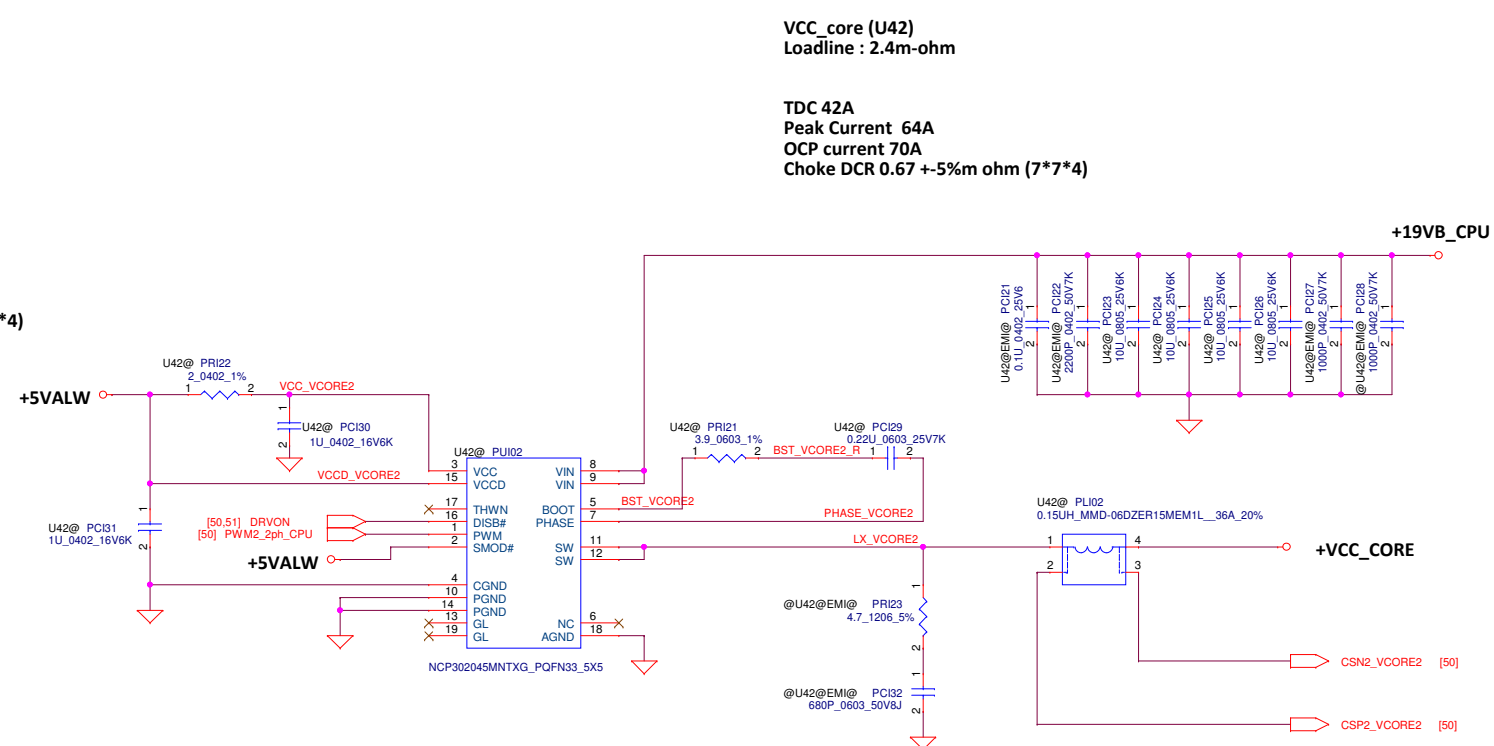
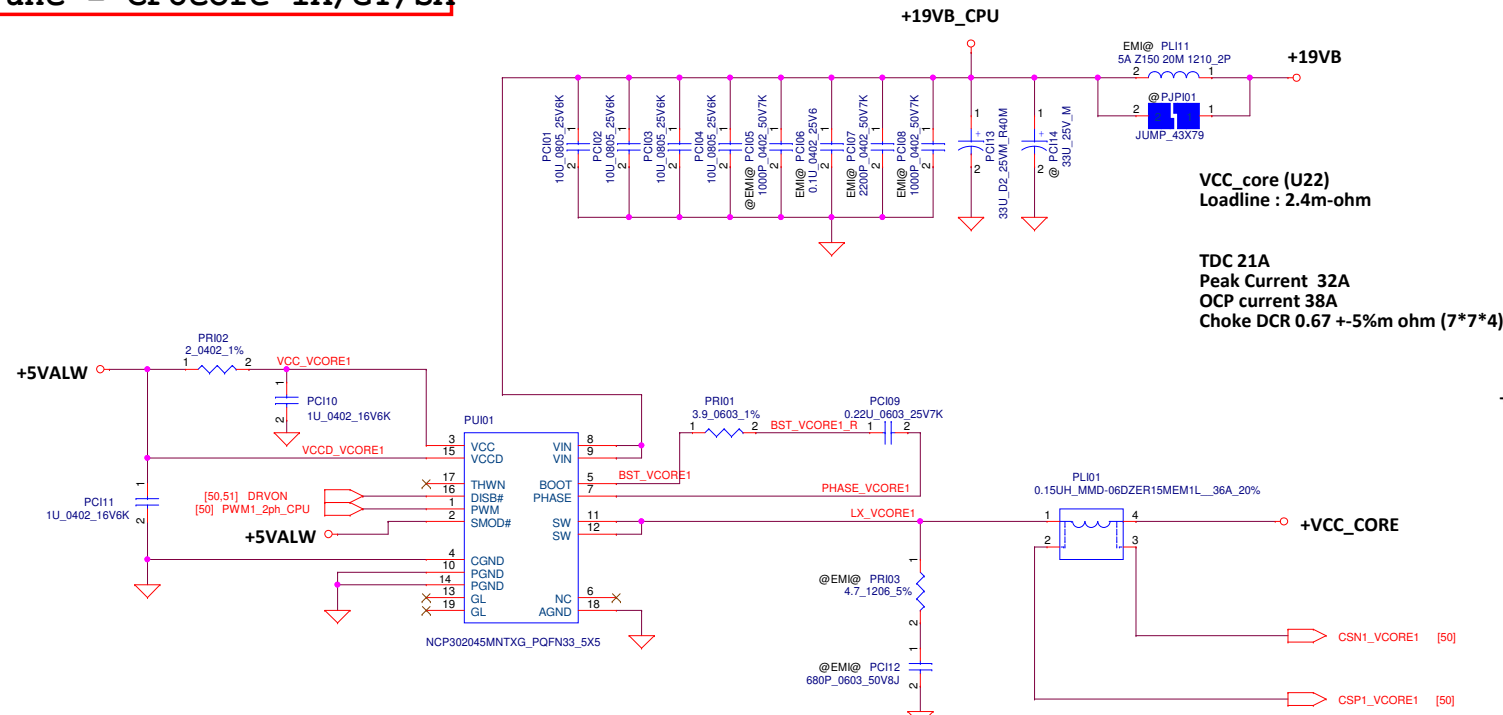
Main Func = CPU



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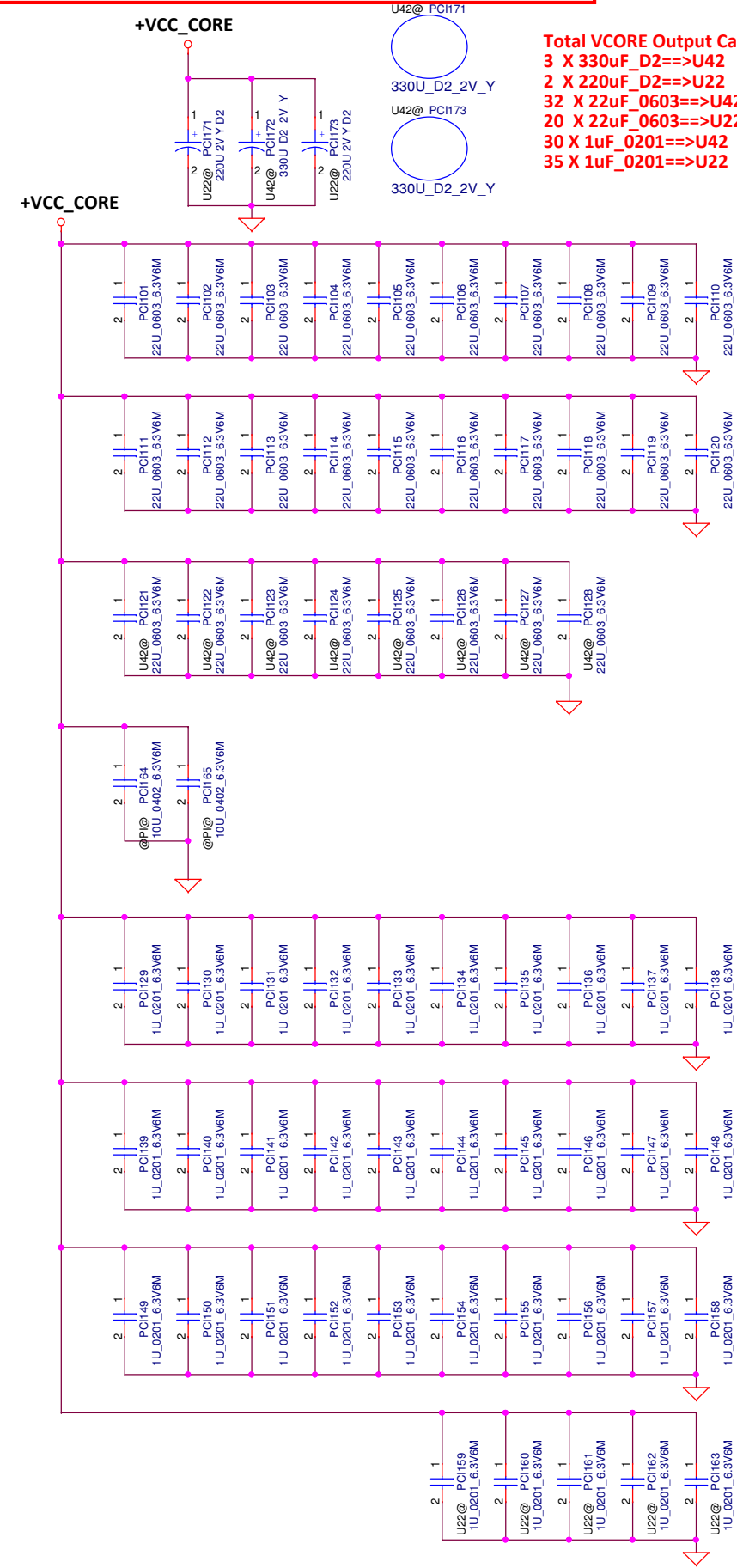
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				PWR_CPU	X00
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Main Func = CPUcore IA/GT/SA

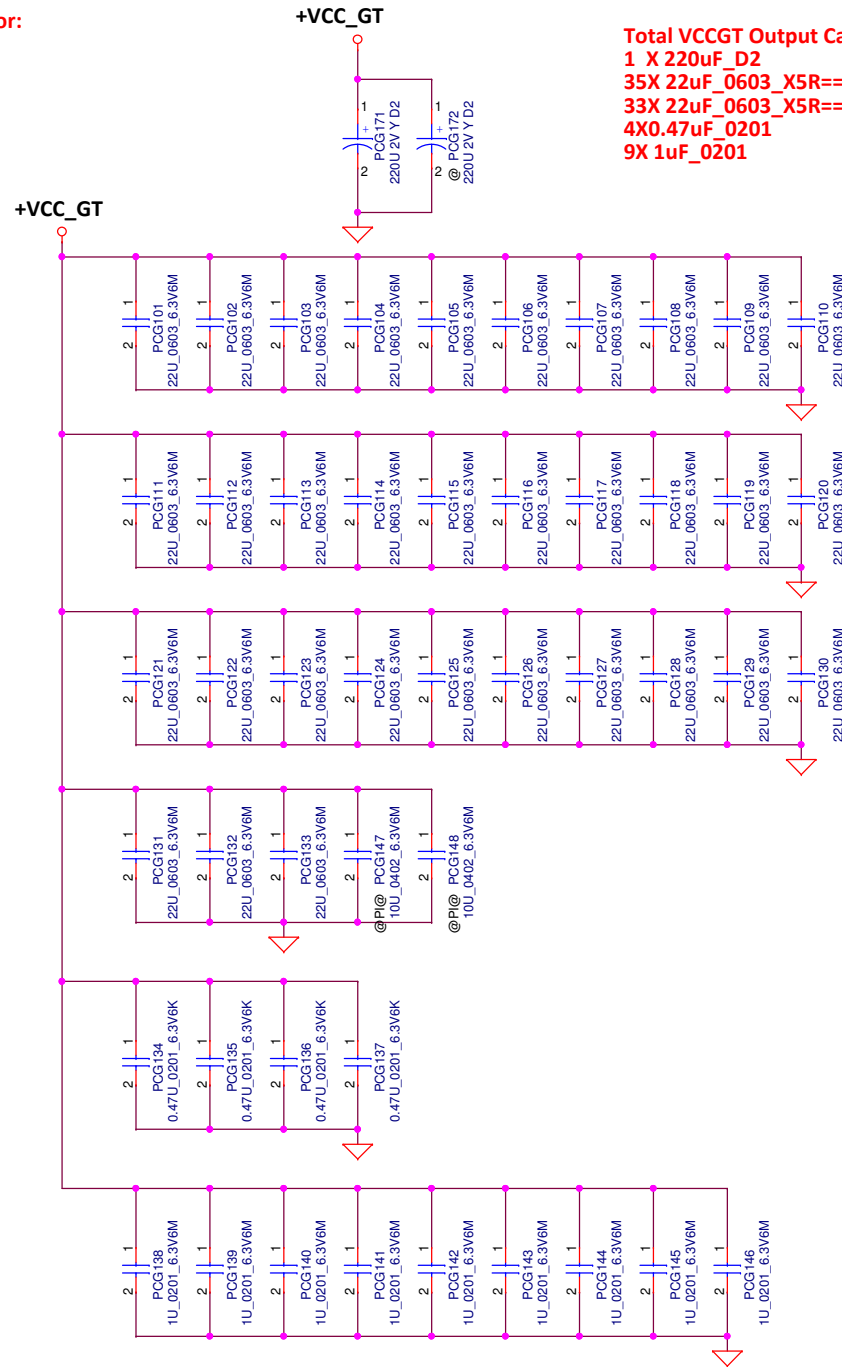


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Issued Date	2015/12/07	Deciphered Date	2017/01/31	Title	PWR CPUcore IA/GT/SA
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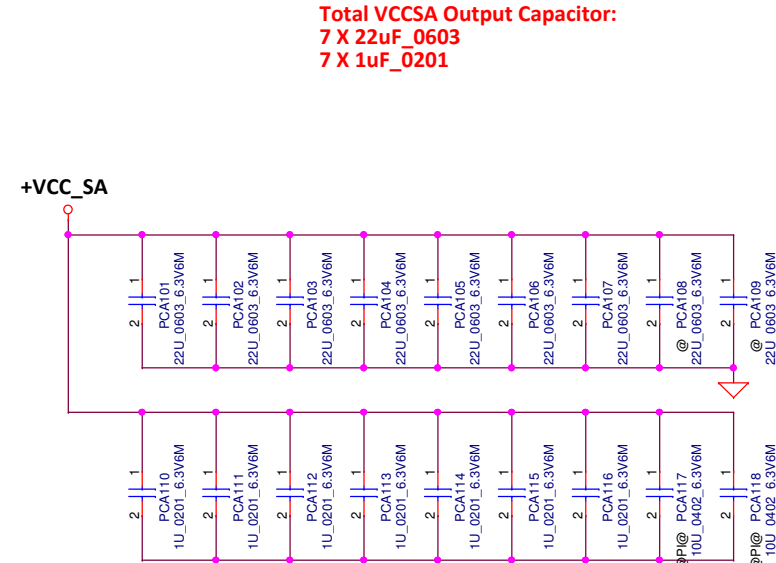
Main Func = CPU/ VGA / SA MLCC



Total VCORE Output Capacitor:  
3 X 330uF\_D2==>U42  
2 X 220uF\_D2==>U22  
32 X 22uF\_0603==>U42  
20 X 22uF\_0603==>U22  
30 X 1uF\_0201==>U42  
35 X 1uF\_0201==>U22

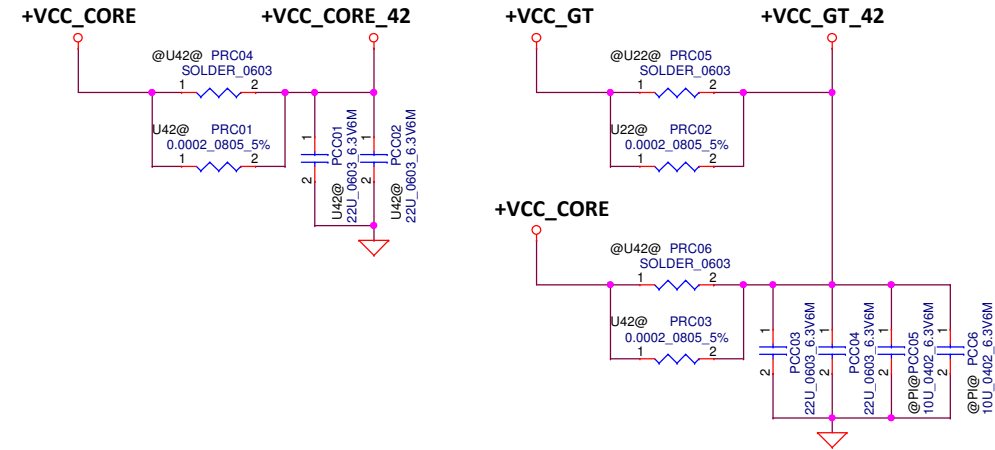


Total VCCGT Output Capacitor:  
1 X 220uF\_D2  
35X 22uF\_0603\_X5R==>U22  
33X 22uF\_0603\_X5R==>U42  
4X0.47uF\_0201  
9X 1uF\_0201



Total VCCSA Output Capacitor:  
1 X 220uF\_D2  
7 X 22uF\_0603  
7 X 1uF\_0201

VCC\_CORE\_42,VCC\_GT\_42 for KBL-R 4+2  
VCC\_GT\_42 colay GT and CORE



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3							
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5							
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7							
8							